IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF COLORADO

REALTIME ADAPTIVE STREAMING LLC, Plaintiff, v. ADVANCED MICRO DEVICES, INC., Defendant.	Case No. 18CV1173 JURY TRIAL DEMANDED

COMPLAINT FOR PATENT INFRINGEMENT

This is an action for patent infringement arising under the Patent Laws of the United States of America, 35 U.S.C. § 1 *et seq.* in which Plaintiff Realtime Adaptive Streaming LLC ("Plaintiff" or "Realtime") makes the following allegations against Defendant Advanced Micro Devices Inc. ("Defendant" or "AMD").

PARTIES

1. Realtime is a Texas limited liability company. Realtime has a place of business at 1828 E.S.E. Loop 323, Tyler, Texas 75701. Realtime has researched and developed specific solutions for data compression. As recognition of its innovations rooted in this technological field, Realtime holds multiple United States patents and pending patent applications.

2. On information and belief, Defendant AMD is a Delaware corporation with a place of business in Santa Clara, California. AMD has regular and established places of business in this District, including, e.g., at 2950 East Harmony Road, Suite 300, Fort Collins, Colorado 80528-9558. AMD offers its products and/or services, including those accused herein of infringement, to customers and potential customers located in Colorado and in this District. AMD may be served with process through its registered agent for service at The Corporation Company, 7700 E. Arapahoe Road, Suite 220, Centennial, Colorado 80112-1268.

JURISDICTION AND VENUE

3. This action arises under the patent laws of the United States, Title 35 of the United States Code. This Court has original subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

4. This Court has personal jurisdiction over Defendant AMD in this action because AMD has committed acts within the District of Colorado giving rise to this action and has established minimum contacts with this forum such that the exercise of jurisdiction over AMD would not offend traditional notions of fair play and substantial justice. Defendant AMD has committed and continues to commit acts of infringement in this District by, among other things, offering to sell and selling products and/or services that infringe the asserted patents.

5. Venue is proper in this district, e.g., under 28 U.S.C. § 1400(b). AMD is registered to do business in Colorado, and upon information and belief, AMD has transacted business in the District of Colorado and has committed acts of direct and indirect infringement in the District of Colorado. AMD has regular and established place(s) of business in this District, as set forth above.

THE PATENTS-IN-SUIT

6. This action arises under 35 U.S.C. § 271 for AMD's infringement of Realtime's United States Patent Nos. 7,386,046 (the "'046 patent"), 8,934,535 (the "'535 patent"), and 9,769,477 (the "'477 patent") (the "Patents-In-Suit").

7. The '046 patent, titled "Bandwidth Sensitive Data Compression and Decompression," was duly and properly issued by the United States Patent and Trademark Office ("USPTO") on June 10, 2008. A copy of the '046 patent is attached hereto as Exhibit A. Realtime is the owner and assignee of the '046 patent and holds the right to sue for and recover all damages for infringement thereof, including past

infringement.

8. The ’535 patent, titled “Systems and methods for video and audio data storage and distribution,” was duly and properly issued by the USPTO on January 13, 2015. A copy of the ’535 patent is attached hereto as Exhibit B. Realtime is the owner and assignee of the ’535 patent and holds the right to sue for and recover all damages for infringement thereof, including past infringement.

9. The ’477 patent, titled “Video data compression systems,” was duly and properly issued by the USPTO on September 19, 2017. A copy of the ’477 patent is attached hereto as Exhibit C. Realtime is the owner and assignee of the ’477 patent and holds the right to sue for and recover all damages for infringement thereof, including past infringement.

COUNT I

INFRINGEMENT OF U.S. PATENT NO. 7,386,046

10. Plaintiff re-alleges and incorporates by reference the foregoing paragraphs, as if fully set forth herein.

11. On information and belief, AMD has made, used, offered for sale, sold and/or imported into the United States AMD products that infringe the ‘046 patent, and continues to do so. By way of illustrative example, these infringing products include, without limitation, AMD’s products/solutions e.g., AMD’s Video Coding Engine, which is a “[F]ixed-function hardware accelerator that supports H.264 AVC, and SVC encoding.” *See e.g.*, http://developer.amd.com/wordpress/media/2013/11/MediaSDK_ User_Guide_1_1_Beta.pdf. AMD integrates Video Coding Engine into all of their GPUs and APUs, such as, e.g., AMD Radeon R9 Series Graphics Cards, AMD Radeon

R7 Series Graphics Cards, AMD Radeon R5 Series Graphics Cards, AMD Radeon HD 6450 Graphics Cards, AMD Radeon HD 7700 Series Graphics Cards, and all versions and variations thereof since the issuance of the '046 patent ("Accused Instrumentalities").

12. On information and belief, AMD has directly infringed and continues to infringe the '046 patent, for example, through its sale, offer for sale, importation, use and testing of the Accused Instrumentalities, which practices the system claimed by Claim 40 of the '046 patent, namely, a system, comprising: a data compression system for compressing and decompressing data input; a plurality of compression routines selectively utilized by the data compression system, wherein a first one of the plurality of compression routines includes a first compression algorithm and a second one of the plurality of compression routines includes a second compression algorithm; and a controller for tracking throughput and generating a control signal to select a compression routine based on the throughput, wherein said tracking throughput comprises tracking a number of pending access requests to a storage device; and wherein when the controller determines that the throughput falls below a predetermined throughput threshold, the controller commands the data compression engine to use one of the plurality of compression routines to provide a faster rate of compression so as to increase the throughput. Upon information and belief, AMD uses the Accused Instrumentalities to practice infringing methods for its own internal non-testing business purposes, while testing the Accused Instrumentalities, and while providing technical support and repair services for the Accused Instrumentalities to AMD's customers.

13. For example, the Accused Instrumentalities utilize H.264 video compression standard, which utilizes Scalable Video Coding technology. See,

e.g., Recommendations ITU-T H.264 (03/2010) Annex G (Scalable video coding), p. 387-599.

Annex G

Scalable video coding

(This annex forms an integral part of this Recommendation | International Standard)

This annex specifies scalable video coding, referred to as SVC.

G.1 Scope

Bitstreams and decoders conforming to one or more of the profiles specified in this annex are completely specified in this annex with reference made to clauses 2-9 and Annexes A-E.

G.2 Normative references

The specifications in clause 2 apply with the following additions.

- ISO/IEC 10646:2003, *Information technology – Universal Multiple-Octet Coded Character Set (UCS)*.
- IETF RFC 3986 (2005), *Uniform Resource Identifiers (URI): Generic Syntax*.

G.3 Definitions

For the purpose of this annex, the following definitions apply in addition to the definitions in clause 3. These definitions are either not present in clause 3 or replace definitions in clause 3.

G.3.1 **arbitrary slice order (ASO)**: A *decoding order* of *slices* in which the *macroblock address* of the first *macroblock* of some *slice* of a *slice group* within a *layer representation* may be less than the *macroblock address* of the first *macroblock* of some other preceding *slice* of the same *slice group* within the same *layer representation* or in which the *slices* of a *slice group* within a *layer representation* may be interleaved with the *slices* of one or more other *slices groups* within the same *layer representation*.

G.3.2 **associated NAL unit**: A *NAL unit* that directly succeeds a *prefix NAL unit* in *decoding order*.

G.3.3 **B slice**: A *slice* that may be decoded using *intra-layer intra prediction* or *inter prediction* using at most two *motion vectors* and *reference indices* to *predict* the sample values of each *block*.

G.3.4 **base layer**: A *bitstream subset* that contains all *NAL units* with the nal_unit_type *syntax element* equal to 1 and 5 of the *bitstream* and does not contain any *NAL unit* with the nal_unit_type *syntax element* equal to 14, 15, or 20 and conforms to one or more of the profiles specified in Annex A.

G.3.5 **base quality layer representation**: The *layer representation* of the *target dependency representation* of an *access unit* that is associated with the quality_id *syntax element* equal to 0.

G.3.6 **bitstream subset**: A *bitstream* that is derived as a *subset* from a *bitstream* by discarding zero or more *NAL units*. A *bitstream subset* is also referred to as *sub-bitstream*.

G.3.7 **bottom macroblock (of a macroblock pair)**: The *macroblock* within a *macroblock pair* that contains the samples in the bottom row of samples for the *macroblock pair*. For a *field macroblock pair*, the bottom macroblock represents the samples from the region of the *bottom field* or *layer bottom field* of the *frame* or *layer frame*, respectively, that lie within the spatial region of the *macroblock pair*. For a *frame macroblock pair*, the bottom macroblock represents the samples of the *frame* or *layer frame* that lie within the bottom half of the spatial region of the *macroblock pair*.

G.3.8 **coded slice in scalable extension NAL unit**: A *coded slice NAL unit* that contains an *EI slice*, *EP slice*, or an *EB slice*.

G.3.9 **complementary reference field pair**: A collective term for two *reference fields* that are in consecutive *access units* in *decoding order* as two *coded fields*, where the *target dependency representations* of the *fields* share the same value of the frame_num *syntax element* and where the second *field* in *decoding order* is not an *IDR picture* and the *target dependency representation* of the second *field* does not include a memory_management_control_operation *syntax element* equal to 5, or a *complementary reference base field pair*.

https://en.wikipedia.org/wiki/Scalable_Video_Coding

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