EXHIBIT A

Consultant Curriculum Vitae

Vojin G. Oklobdzija, Ph.D., IEEE Life Fellow

Professor Emeritus, University of California
Past-President, IEEE Circuits and Systems Society, 2014, 2015
(Phonetic spelling: Vo-in Oklob-j-a)

Contact:

Address:
1285 Grizzly Peak Blvd, Berkeley, CA 94708

Telephone and email:
510-230-3267; vojin@ieee.org, vojin@acsel-lab.com, vojin@integration-corp.com

Expertise

- Computer System Design and Computer Architecture
- VLSI Circuits and Systems
- System Clocking and Clocked Storage Elements
- Logic Design and Machine Organization
- Low-Power Design and Technology
- Computer Arithmetic: VLSI adders, multipliers arithmetic, crypto processors
- Microprocessor Design
- Design for Testability and Fault-Tolerant Computer Design

Professional Summary

Expert witness with 23 years of experience, provided testimony in civil jury trial, and ITC court in Washington, D.C. Provided ten deposition testimonies, written over 30 expert reports on infringement, claim construction, participated in patent review.
Over 40 years of experience in computer and semiconductor industry and 28 years of consulting experience for most major computer and semiconductor companies in the USA and abroad.
Twenty years in academic position, reaching the highest Full Professor level in five years and IEEE Fellow, followed by IEEE Life Fellow (highest) level in engineering profession.

Consultant Curriculum Vitae

Employment History:

From:	2018	**SambaNova Systems Inc.**
To:	on	Palo Alto, California
	Position:	Senior Principal Engineer
		Machine Learning: Processor design and development. Responsible for the Arithmetic Unit.
From:	2016	**Esperanto Technologies Inc**
To:	2018	Mt. View, California
	Position:	Founding Member
		Massively parallel, ultra-low-power microprocessor system development. Working on low-power and low-voltage design in order to achieve minimal power operation for a given performance.
From:	2013	**Silicon Analytics Inc.**
To:	on	San Jose, California
	Position:	Founder and President
		Expertise and tool development for power optimization. Targeting low and ultra-low power design.
From:	2013	**Skyera Inc.**
To:	2014	San Jose, California
	Position:	*Senior Director, Processor Development*
		Design of a massively parallel processor supporting Solid-State, Peta-Byte storage array. Managing entire processor design team.
From:	1996	**Integration Corp.**
To:	Present	Berkeley, California
	Position:	President and CEO
		Processor design services: Developed fastest encryption processor for Blue Steel Networks (sold to Broadcom for $150M). Designed and developed network encryption processor for Digital Archways. Design and developed Media and Floating-Point Processor for BOPS Inc.
From:	1992	**Advanced Computer Systems Engineering Laboratory**
To:	Present	Currently: Berkeley, California
	Position:	*Director*
		Conducting research in: Low-Power systems and processor development with implementations in multi-media, cryptography and wireless communication. Developed a comprehensive family of clocked storage elements and clocking strategies for high performance and low-power applications; optimization method for digital circuits and system design resulting in up to 50% energy savings; the fastest parallel multiplier, adder and method for generation, estimation and comparison of arithmetic structures.
From:	1991	**University of California Davis**
To:	Present	Davis, CA
	Position:	Professor Emeritus, 2006-Present

Consultant Curriculum Vitae

1991-2006: Full Professor, Electrical and Computer Engineering Department

From: 2007 **University of Texas at Dallas**
To: 2010 Dallas, TX
Position: *Visiting Professor;* Director of Systems and Circuits Group (2007-2010), *Adjunct Professor (2010 – 2012)*

From: 2005 **Sydney University**
To: 2007 Sydney, Australia
Position: *Computer Engineering Chair and Chair Professor, Department of Electrical and Information Engineering*
(ARC funding $1,900,000).

From: 03/2004 **Ecole Polytechnique Federale de Lausanne, EPFL**
To: 10/2004 Lausanne, Switzerland
Position: *Visiting Professor, Processor Architecture Laboratory*
Developed and taught a new doctoral course in computer arithmetic

From: 07/2003 **Government of Korea**
To: 12/2003 Seoul, Korea
Position: *Distinguished Visiting Professor,* Korea Information Technology Assessment Program
Established research program in digital media and secured a three year grant in *"Power Minimization for Media Signal Processing"* from the Korean government (appx: $300,000). Established and taught the course titled: *"Digital System Engineering".*

From: 1998 **University of California at Berkeley**
To: 1990 Berkeley, CA
Position: *Visiting IBM Faculty, Electrical Engineering and Computer Science Department*
Teaching: *Upper level courses:* CS150 Digital System Design, CS152: Computer System Design and Organization. *Graduate courses:* CS252 Computer System Architecture, CS292I VLSI Implementation of Fast Computer Arithmetic. Assisted in preliminary evaluation and preparation of Patterson-Hennessy book "Computer Architecture: A Quantitative Approach".

From: 1996 **Siemens Corporation**
To: 1998 San Jose, CA
Position: Architecture / Circuit Design Manager
Development of Full-Custom high-performance arithmetic units. Chief architect for Siemens / Infineon TriCore line of integrated RISC-DSP controller. Development of and embedded Logic-DRAM processor (32-bit, RISC + DSP). Managed a group of 15 engineers.

From: 1982 **IBM T.J. Watson Research Center**
To: 1991 Yorktown Heights, NY
Position: *Research Staff Member*
My work was in the areas of: *Systems and Architecture, CPU and Floating-*

Point processor design, Circuit design, Design for Testability
Development and implementation of VLSI RISC architectures:
1. High Performance 801 (first RISC microprocessor) for PC-RT (ROMP-E project).
2. Very high performance Super-Scalar RISC Architecture, RS/6000: floating point processor and system organization. (current PowerPC architecture)
3. Architectural definition and design of VLSI-RISC type processor to be used in a highly parallel super-computer. IBM SP-2.

From: 1979 **Xerox Corp.**
To: 1982 El Segundo, CA
Position: *Member of the Engineering Staff, Microelectronics Center*
Work on the VLSI microprocessors design and diagnostic. Chip set for the first Workstation – Xerox Alto.

From: 1977 **UCLA**
To: 1982 Los Angeles, CA
Position: *Research Assistant & Senior Research Engineer, Computer Science Department*
Worked on VLSI Design and Testability, VLSI Design Methodology, Fault-Tolerant Computer Design and High Reliability, Computer Arithmetic and Design of Arithmetic Processor.

From: 1974 **University of Belgrade**
To: 1976 Belgrade, Yugoslavia
Position: *Assistant Professor, Electrical Engineering Department*
Research and teaching in Analog and Digital Electronics.

From: 1973 **Institute for Automation and Telecommunications**
To: 1974 Belgrade Yugoslavia
Position: *Research Engineer*
Design of non-standard analog circuitry for the analog part of the state of the art hybrid computer (project with USSR). Design of an Analog Multiplier based on Time Division Concept.

From: 1971 **Institute of Physics**
To: 1973 Belgrade Yugoslavia
Position: *Research Physicist*
Experimental work in plasma physics with extensive use of computer tools for simulation and data acquisition. Written software in Fortran on IBM 360/44 and CDC 6600.

Current and Past Professional Service:

- Past-President, IEEE Circuits Systems Society
- President, IEEE Circuits and Systems Society (2014, 2015)
- President Elect, IEEE Circuits and Systems Society (2013).
- Vice President, Technical Activities, IEEE Circuits and Systems Society (2009-2013)
- General Chair: International Symposium on Low-Power Electronics, 2010.

DOCKET ALARM

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts

Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research

With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips

Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS
Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS
Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS
Sync your system to PACER to automate legal marketing.