EXHIBIT 9

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EFLX® Embedded FPGA

Dense, Fast, Proven, Scalable

flexlogix EFLX embedded FPGA ®

Everything You Need for an eFPGA in Your SoC

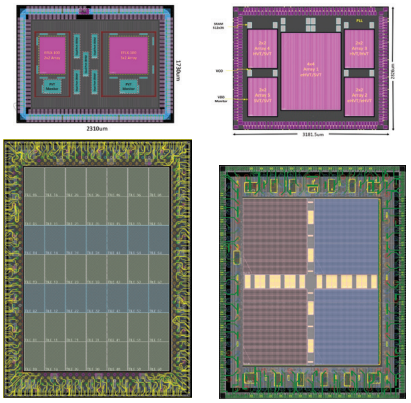
- ✔ High density similar to full custom FPGA
- ✔ High performance similar to full custom FPGA
- ✔ eFPGA IP Core silicon proven
- ✔ eFPGA Arrays of any size by tiling proven eFPGA IP cores to the size needed
- ✔ Options for DSP and RAM as you need
- ✔ Available and silicon proven in TSMC 16, 28, 40 & on demand for any TSMC node
- ✔ Compatibility with your metal stack and your voltage range
- ✔ Software tools with a Graphical User Interface
- ✔ Timing files extracted from design database and available across all corners
- ✔ DFT fault coverage of 99% with special logic for 100x acceleration of test time

TSMC IP Alliance Member

Flex Logix® is now a TSMC IP Alliance Member based on the work it has done with TSMC over the past several years to develop embedded FPGA IP meeting TSMC's standards for documentation, design methodology, and engineering validation in silicon. Flex Logix will continue to prove all EFLX® embedded FPGA IP in silicon after rigorous engineering checks and sign-offs.

TSMC 40/28/16, GF 14, Sandia 180, others in 6 mo.s

TSMC 16FF+/FFC	EFLX150 Gen 2	*PROVEN IN SILICON*
TSMC 16FF+/FFC	EFLX4K Gen 2	*PROVEN IN SILICON*
TSMC 28HPM/HPC	EFLX2.5K Gen 1	*PROVEN IN SILICON*
TSMC 28HPC/HPC+	EFLX4K Gen 2	In fabrication
TSMC 40ULP/LP	EFLX 100 Gen 1	*PROVEN IN SILICON*
GF 14LPP	EFLX4K Gen 2	In design
Sandia 180	EFLX4K Gen 2	In fabrication

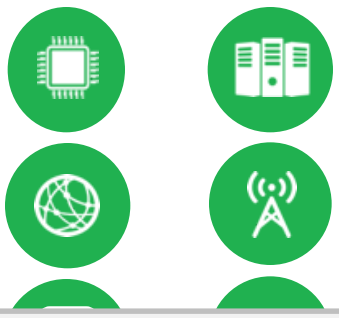


Detailed product briefs are available for each EFLX core. Operating temperature range is -40C to +125C Tj. Multiple voltage ranges are supported. The EFLX Compiler has timing at numerous corners for each core. We an port to other foundries/process nodes in ~6 months.

Multiple Customers and Markets Adopting eFPGA

Multiple customers have built chips using EFLX eFPGA and more are in design. Customers include DARPA, Harvard, HiPer, Sandia, SiFive & more. Markets and value propositions include:

SoCs, ML, Vision	Reconfigurable accelerators & algorithm iteration in real time.
Networking	Reconfigurable switches, NICs, etc which can be updated for changing protocols and needs.
Data Center	Accelerators and Processor+FPGA integration.
Base Stations	Reconfigurable DFE integrated for lower power and higher performance.



EFLX Embedded FPGA

XFLX™, ArrayLinx™ & RAMLinx™ Interconnects

Revolutionary Interconnect Enables Density and Scalability

Traditional FPGA fabrics are only 20% programmable logic: the programmable interconnect takes 80% of the area!

Flex Logix has developed revolutionary new interconnects:
1. XFLX Interconnect: reduces the programmable interconnect area required by about 1/2 AND reduces the number of metal layers required. This enables density similar to full custom FPGA and compatibility with most metal stacks.
2. ArrayLinx Interconnect: this allows a large number of eFPGA array sizes to be built quickly using a single, silicon proven eFPGA IP core.
3. RAMLinx Interconnect: this allows any type and amount of RAM to be quickly interleaved in an eFPGA array using silicon proven eFPGA IP cores.

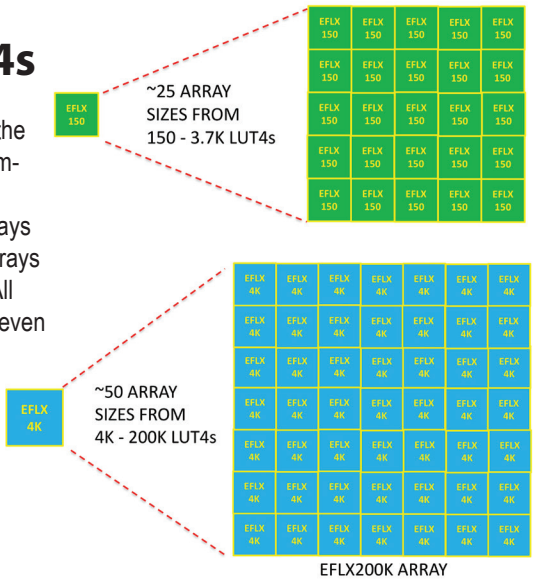
These interconnects are covered by numerous issued and pending patents in the USA and other countries.

Density & Performance Similar to Full Custom FPGA

The XFLX interconnect takes ~1/2 the area of traditional FPGA mesh interconnect, so even though we use standard cells, for rapid implementation, we achieve density and performance similar to full custom FPGA. And we use only 5-7 metals layers, so we are compatible with most metal stacks.

Embedded FPGAs from 150 LUTs to ~200K LUT4s

EFLX arrays are constructed from one of two building blocks: the EFLX150 core with ~150 LUT4s and the EFLX4K core with ~4K LUT4s. Both are complete embedded FPGAs with programmable logic, programmable interconnect, I/O, clock circuitry and configuration logic. They also have a top level ArrayLinx Interconnect which is used to build arrays of larger size by "tiling" into arrays with no GDS change. Arrays of different sizes can be delivered in days & customers are encouraged to use multiple, different size arrays in a single design. The LUTs in our Gen 2 architecture are 6-input LUTs for higher speed and density. All EFLX cores are proven in silicon in arrays of at least 2x2 so all array sizes are proven out. If you need even larger arrays, ask about our roadmap to ~800K LUT4 arrays.

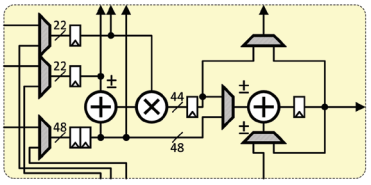


Thousands of Interface Pins

A single EFLX4K core has >1000 interface pins: 632 in and 632 out; larger arrays have much more. You can connect EFLX embedded FPGAs into wide, fast buses and wide data and control paths; the interfaces are standard CMOS so they run very fast.

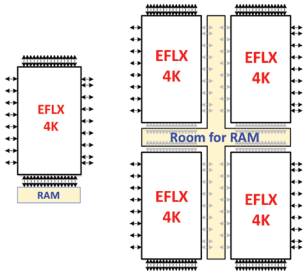
Optional MACs for DSP/AI/ML Acceleration

Both the EFLX-100/150 and EFLX4K cores are offered in versions where some of the LUTs are replaced with Multiplier-Accumulator (MAC) blocks consisting of a 22-bit pre-adder, 22-bit multiplier and 48-bit accumulator which can be pipelined for very fast DSP implementations. For AI/ML, the multiplier can be configured as two 11x11 multipliers for double the throughput.



Optional RAM: Any Kind, Any Amount

The EFLX cores contain memory. If you require more, it can be synthesized at the edge of the array or between the cores, within the array. The EFLX Compiler software will map your RTL onto the RAM as part of the array. We synthesize RAM from standard compilers with optional MBIST: single port or dual port, whatever size and number of blocks you want, with or without parity/ECC. We can also integrate your special memory like TCAM or custom accelerators.

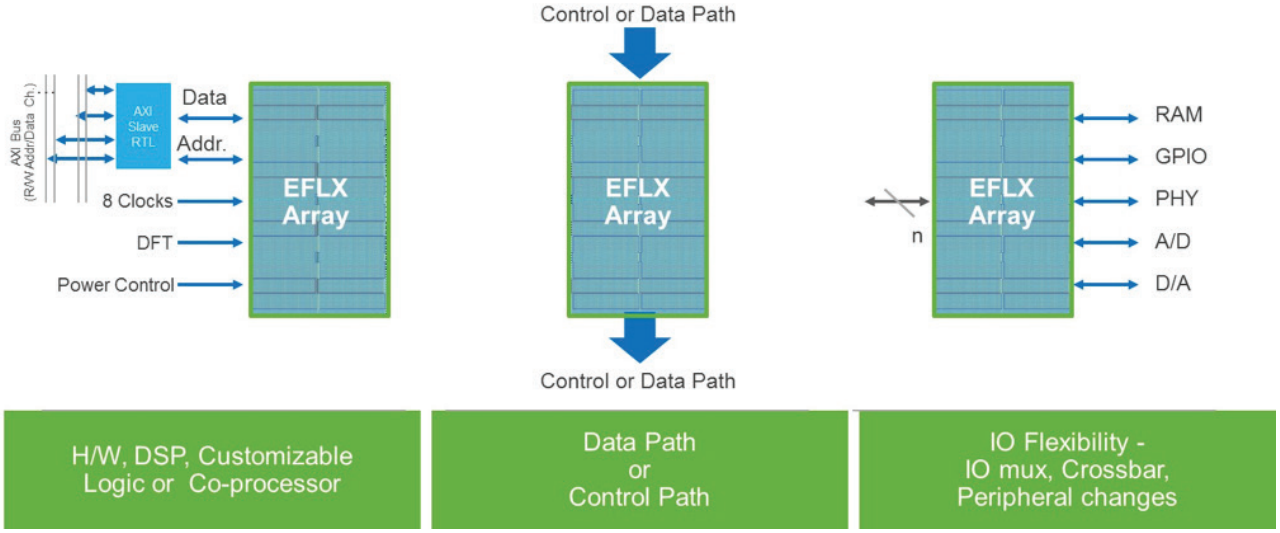


Test and Reliability Features

EFLX Embedded FPGA

Integration & Programming

Flex Logix has interface RTL for AXI, AHB and APB buses as a Slave or Master.



Design Deliverables

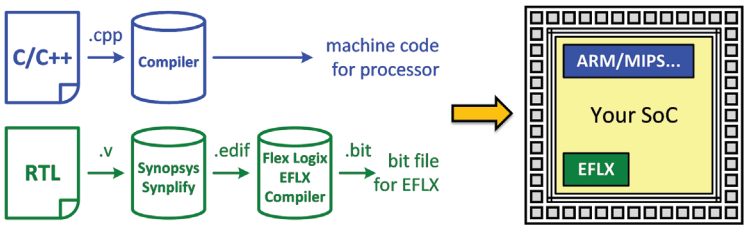
We deliver the exact EFLX array size you specify, your mix of all-LUT and LUT-DSP cores, and RAM if needed. If you want multiple arrays of different sizes/configurations we can easily accommodate that. If your requirements change mid-design we can quickly deliver a larger or smaller array.
The design files we deliver are: LEF, LIB, Verilog™ Model, SDF, GDS-II™, CDL/Spice netlist, and DFT test vectors (>>98.5% coverage).
We designed and built a validation chip which is proven in silicon using these same files.

Power Management Modes & IR Drop Analysis

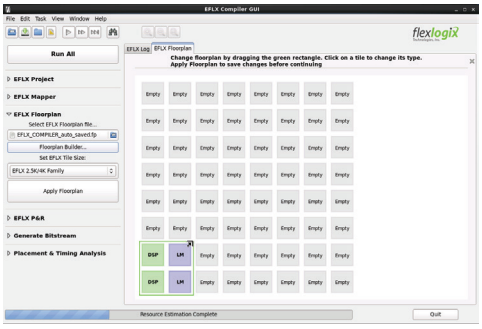
EFLX cores can be power-gated to reduce static power if not in use; in TSMC 40ULP we added more power management modes and 0.5V state retention.
We use EDA tools to analyze the EFLX array for IR drop in static & high-switching activity dynamic modes to ensure it can operate reliably in your SoC.

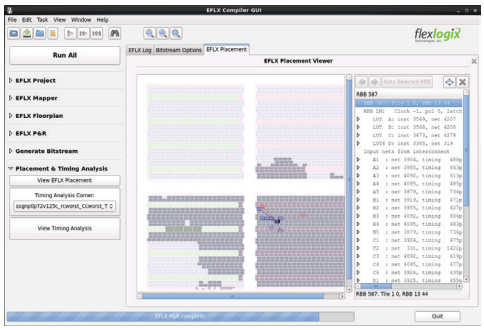
EFLX Compiler Programming

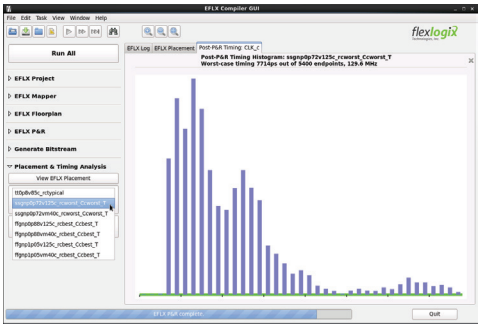
To program the EFLX array, use Synopsys® Synplify or another synthesis tool to generate an .edif file which is then input to the EFLX Compiler. You also provide an IO file which shows how the EFLX array is connected to the rest of your chip. EFLX Compiler packs, places, routes and iterates to generate optimum timing performance: if it is acceptable, EFLX Compiler generates the bitstream which when loaded into the EFLX array makes it execute your RTL.



Our GUI makes array floorplan building and timing path analysis quick and easy. New features are in development as well.







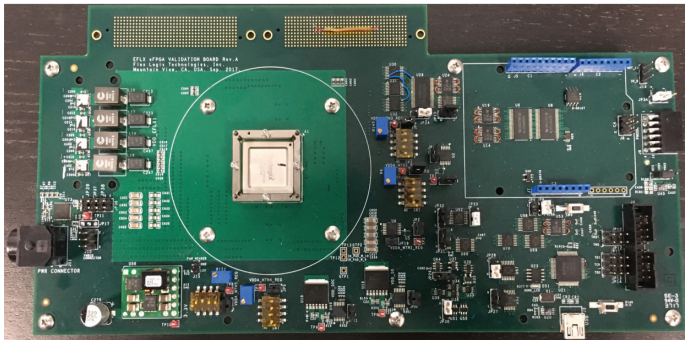
Assistance Throughout Your Chip Evaluation and Design

EFLX Embedded FPGA
Evaluation Boards & Business

flexlogix
EFLX embedded FPGA

EFLX200K T16FFC+ Evaluation Board

Our most recent validation chip for TSMC16FFC+ EFLX4K implemented a full 7x7 array, the EFLX200K is also designed as a customer evaluation chip and is now available on an evaluation board. The EFLX200K has 182K LUT4, 560 MACs, 1.4Mbit attached SRAM, PLLs and PVT monitors. Using this customer can load even very large RTL to verify performance at full speed and at different temperatures and voltages; also customers can measure static and dynamic power. All future validation chips (up next is the TSMC28HPC+) will also be featured on evaluation boards for customer use.



Business Model

We have a competitive advantage: we can give you the exact eFPGA you need in any TSMC process node/variant, in the size you want, with the options you want and we can deliver it off the shelf already in multiple nodes and in ~6 months for any other TSMC node. And what we deliver is as dense and fast as full custom FPGA. Plus we can do this with less engineering-months than our competitors. We have done more ports in less time than our competitors.

So we can afford to be flexible and very competitive on pricing. On ports to new TSMC nodes we don't charge you for development: we price it the same as if it were already off the shelf.

Our typical business model for a single design is: A) a license fee for any number and size/configuration of eFPGAs on your chip typically paid in milestones: contract, IP delivery, working silicon, B) a small royalty, pennies per chip, C) an annual seat license fee for the EFLX Compiler. We are open to other structures as well.

Proven Management

Our CEO was a GM at AMD since 1983 ending up as Senior VP of processors; then was founding CEO of Rambus joining as the 4th employee, achieving IPO 7 years later and running the company until it reached $2 Billion in Market Capitalization. Our Silicon Engineering VP, Sales VP and Director of Solutions Architecture all have >20 years experience at firms like ARM, Intel, and Rambus. Our Software Director has >10 years experience at Synopsys and did his PhD thesis on FPGA Place & Route. Our Sr. Hardware Design Manager has >10 years experience at Oracle designing in processes down to 7nm. Our Hardware Design Manager has done 8 FPGA/eFPGA designs.

Well Financed

LUX eclipse

We have raised ~$15 Million from Lux Ventures, Eclipse Capital & SVB.
We have a strong cash balance. Our investors have deep pockets for additional capital as needed.
We are committed to keep up with growing customer demand and to invest as necessary to do so.