EXHIBIT 8

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(12) **United States Patent**
Konda

(10) **Patent No.: US 10,050,904 B2**
(45) **Date of Patent: *Aug. 14, 2018**

(54) **VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED AND PYRAMID NETWORKS WITH LOCALITY EXPLOITATION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 10 days.

This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

(63) Continuation of application No. 14/522,599, filed on Oct. 24, 2014, now Pat. No. 9,529,958, which is a (Continued)

(51) **Int. Cl.**

G06F 17/50	(2006.01)
H04L 12/933	(2013.01)
H04L 12/50	(2006.01)

(52) **U.S. Cl.**

CPC ***H04L 49/1507*** (2013.01); ***G06F 17/5054*** (2013.01); ***G06F 17/5077*** (2013.01); ***H04L 12/50*** (2013.01); ***H04L 49/10*** (2013.01)

(58) **Field of Classification Search**

CPC G06T 15/005; G06T 1/20; G06T 1/60; G06T 5/002; G06F 17/5054; G06F 3/017;

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(56) **References Cited**

U.S. PATENT DOCUMENTS

5,153,843 A 10/1992 Batcher
5,451,936 A 9/1995 Yang et al.

(Continued)

OTHER PUBLICATIONS

Guy Lemieux et.al., Generating highlyroutablesparse crossbars for PLDs. In ACMISIGDA Int'l. Symposium on Field Programmable Gate Arrays, pp. 155-164, Monterey, CA, Feb. 2000.

(Continued)

Primary Examiner — Binh Tat

(57) **ABSTRACT**

VLSI layouts of generalized multi-stage and pyramid networks for broadcast, unicast and multicast connections are presented using only horizontal and vertical links with spacial locality exploitation. The VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa. Furthermore the shuffle exchange links are employed between different sub-integrated circuit blocks so that spacially nearer sub-integrated circuit blocks are connected with shorter links compared to the shuffle exchange links between spacially farther sub-integrated circuit blocks. In one embodiment the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power and full connectivity with significantly fast compilation.

The VLSI layouts with spacial locality exploitation presented are applicable to generalized multi-stage and pyramid networks, generalized folded multi-stage and pyramid networks, generalized butterfly fat tree and pyramid networks, generalized multi-link multi-stage and pyramid networks, generalized folded multi-link multi-stage and pyramid networks, generalized multi-link butterfly fat tree and pyramid

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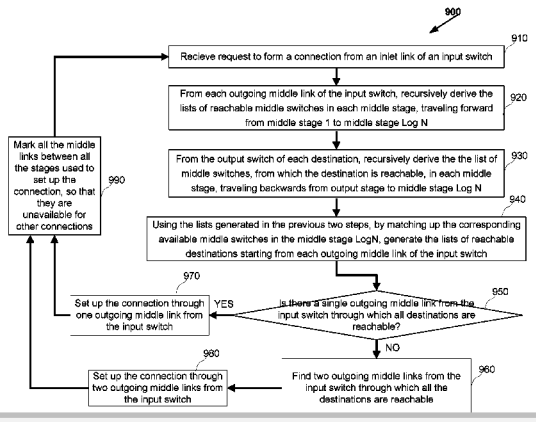

networks, generalized hypercube networks, and generalized cube connected cycles networks for speedup of s≥1. The embodiments of VLSI layouts are useful in wide target applications such as FPGAs, CPLDs, pSoCs, ASIC placement and route tools, networking applications, parallel & distributed computing, and reconfigurable computing.

20 Claims, 43 Drawing Sheets

Related U.S. Application Data

continuation of application No. 13/502,207, filed as application No. PCT/US2010/052984 on Oct. 16, 2010, now Pat. No. 8,898,611.

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(58) **Field of Classification Search**
CPC G06F 17/5077; G06F 15/7867; G06F 15/8015; G06F 19/24; G06F 19/345; G06F 1/163; G06F 3/00; G06F 3/0325; G06F 3/042; G06F 3/04842; G06F 3/04845; G06F 3/0425; G06F 17/509; G06F 19/702
USPC 716/126–132
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,018,523	A	1/2000	Even	
6,185,220	B1	2/2001	Muthukrishnan et al.	
6,335,930	B1 *	1/2002	Lee	H04L 49/101 370/387
6,940,308	B2	9/2005	Wong	
8,170,040	B2	5/2012	Konda	
8,269,523	B2	9/2012	Konda	
8,270,400	B2	9/2012	Konda	
8,363,649	B2	1/2013	Konda	
8,898,611	B2 *	11/2014	Konda	G06F 17/509 716/121
9,529,958	B2	12/2016	Konda	
2012/0269190	A1 *	10/2012	Konda	G06F 17/5054 370/388
2014/0313930	A1 *	10/2014	Konda	H04L 49/1515 370/254
2015/0049768	A1 *	2/2015	Konda	H04L 49/1515 370/411

OTHER PUBLICATIONS

S. Sivaswamy et. al., "HARP: hard-wired routing pattern FPGAs", FPGA'05, Monterey, California, USA, Feb. 20-22, 2005.
Yeh, C.-H., E.A. Varvarigos, and B. Parhami, "Efficient VLSI layouts of hypercubic networks," Proc. Symp. Frontiers of Massively Parallel Computation, Feb. 1999.
Bhatt, S. N. and Leighton, F. T. 1984. A framework for solving VLSI graph layout problems. J. Comput. Syst. Sci. 28, 300-343.
C. Clos, "A Study of Non-Blocking Switching Networks," Bell System Technical Journal, 32:406-424, 1953.
A. DeHon, "Balancing Interconnect and Computation in a Reconfigurable Computing Array," ACM Int. Symp. on FPGA, pp. 69-78, Feb. 1999.
Chihming Chang, Rami Melhem, "Arbitrary Size Benes Networks", Hoda El-Sayed and Abdou Youssef; "The r-truncated Benes Networks and their Randomized Routing Algorithms" 1997 Intl Conf on Parallel and Dist Sys, Seoul, Korea, Dec. 1997.
Guy Lemieux and David Lewis, "Using Sparse Crossbars within LUT Clusters", Procds of the ACM/SIGDA Intl Symp on Field Prog Gate Arrays 2001, Feb. 11-13, 2001, Monterey, CA.
P. Manuel, W. K. Qureshi, A. William, A. Muthumalai, "VLSI layout of Benes networks,", J. of Discrete Math. Sci. & Cryptography, vol. 10, No. 4, pp. 461-472, 2007.
Quinn, Michael J, "Parallel Computing: Theory and Practice", 2nd. ed., 1994, McGraw Hill Series in computer Science, Networks, and parallel computing, ISBN 0-07-051294-9.
Ronald I. Greenberg, "The Fat-Pyramid and Universal Parallel Computation Independent of wire delay" IEEE Trans. Computers, 43(12):1358-1364, Dec. 1994.
Hypertree: A Multiprocessor Interconnection Topology , by James R. Goodman and Carlo H Sequin, Computer Science Technical Report #427, Dept , of EECS, University of California.
Data Movement Techniques for the pyramid computer, Russ Miller and Quentin F. Stout, SIAM Journal on Computing, vol. 16, No. 1, pp. 38-60, Feb. 1987.
Ivo Dobbelaere, Mark Horowitz, and Abbas El Gamal. Regenerative feedback repeaters for programmable interconnections. IEEE Journal of Solid-State Circuits, 30(11), 1995.
F. Petrini et. al., k-ary n-trees: High performance networks for massively parallel architectures, in: Proceedings of the 11th Intl Parallel Proc. Symp. , IPPS'97, pp. 87-93.
P.Pande et al. "Evaluation of MP-SoC Interconnect Architectures: a Case Study", Proceedings of 4th IWSOC, Banff, Alberta, Canada, Jul. 19-21, 2004.
Yeh, C.-H., Varvarigos, E.A., Parhami, B.: Multilayer VLSI layout for interconnection networks. In: Proc. Intl. Conf. on Parallel Processing, 2000.
M. Lin, A. El Gamal, "A Low-Power Field-Programmable Gate Array Routing Fabric," IEEE Transactions on Very Large Scale Integration, vol. 17, No. 10, pp. 1481-1494, Oct. 2009.
Avior, A et. al., A Tight Layout of the Butterfly Network. Proc. 8-th Annual ACM Symp. on Parallel Alg. and Arch. (SPAA '96), ACM Press Ed., 1996, pp. 170-175.
A. El Gamal et. al., "An Architecture for Electrically Configurable Gate Arrays," IEEE Jrnl of Solid-State Circuits, vol. 24, No. 2, pp. 394-398, Apr. 1989.
Vaughn Betz et. al., Directional bias and non-uniformity in FPGA global routing architectures. In IEEE/ACM Intl. Conference on Computer-Aided Design, pp. 652-659, san jose, 96.
W. Tsu et. al., "HSRA: High-Speed, Hierarchical Synchronous Reconfigurable Array," in Procds. of the Intl. Symp. on Field-Programmable Gate Arrays, Feb. 1999, pp. 125-134.
André DeHon. Rent's Rule Based Switching Requirements. In System-Level Interconnect Prediction (SLIP 2001), pp. 197-204, Mar. 31-Apr. 1, 2001.
A. DeHon, "Unifying Mesh- and Tree-Based Programmable Interconnect," IEEE Trans. on Very Large Scale Int. Systems, vol. 12, No. 10, pp. 1051-1065, Oct. 2004.
Guy Lemieux and David Lewis. Analtyical framework for switch block design. In Intl. Conference on Field Programmable Logic and Applications, pp. 122-131, Sep. 2002.
Chen, G; Lau, FCM, "A tight layout of the cube-connected cycles", The 4th International Conference on High Perf. Computing, Bangalore, India, Dec. 18-21, 1997, p. 422-427.
Michael Shyu, Yu-Dong Chang, Guang-Ming Wu, and Yao-Wen Chang, Generic universal switch blocks. IEEE Transactions on Computers,49(4):348-359, Apr. 2000.
Y. Yamada, et. al. , "Folded Fat H-Tree: an interconnection topology for Dynamically Reconfigurable Processor Array", Embed and Ubiq. Cmpting, Intl Conf. EUC 2004.
A. DeHon. Balancing Interconnect and Computation in a Reconfigurable Computing Array (or, why you don't really want 100% LUT utili). In Proc. of intl. symp. on FPGAs, Feb. 1999.
André DeHon. Compact, Multilayer Layout for Butterfly Fat-Tree.

(56) **References Cited**

OTHER PUBLICATIONS

V. P. Roychdowdhury et. al., "Segmented Channel Routing," IEEE Trans on Computer-Aided Design of Integrated Circuits and Systems, vol. 12, No. 1, pp. 79-95, Jan. 1993.

* cited by examiner

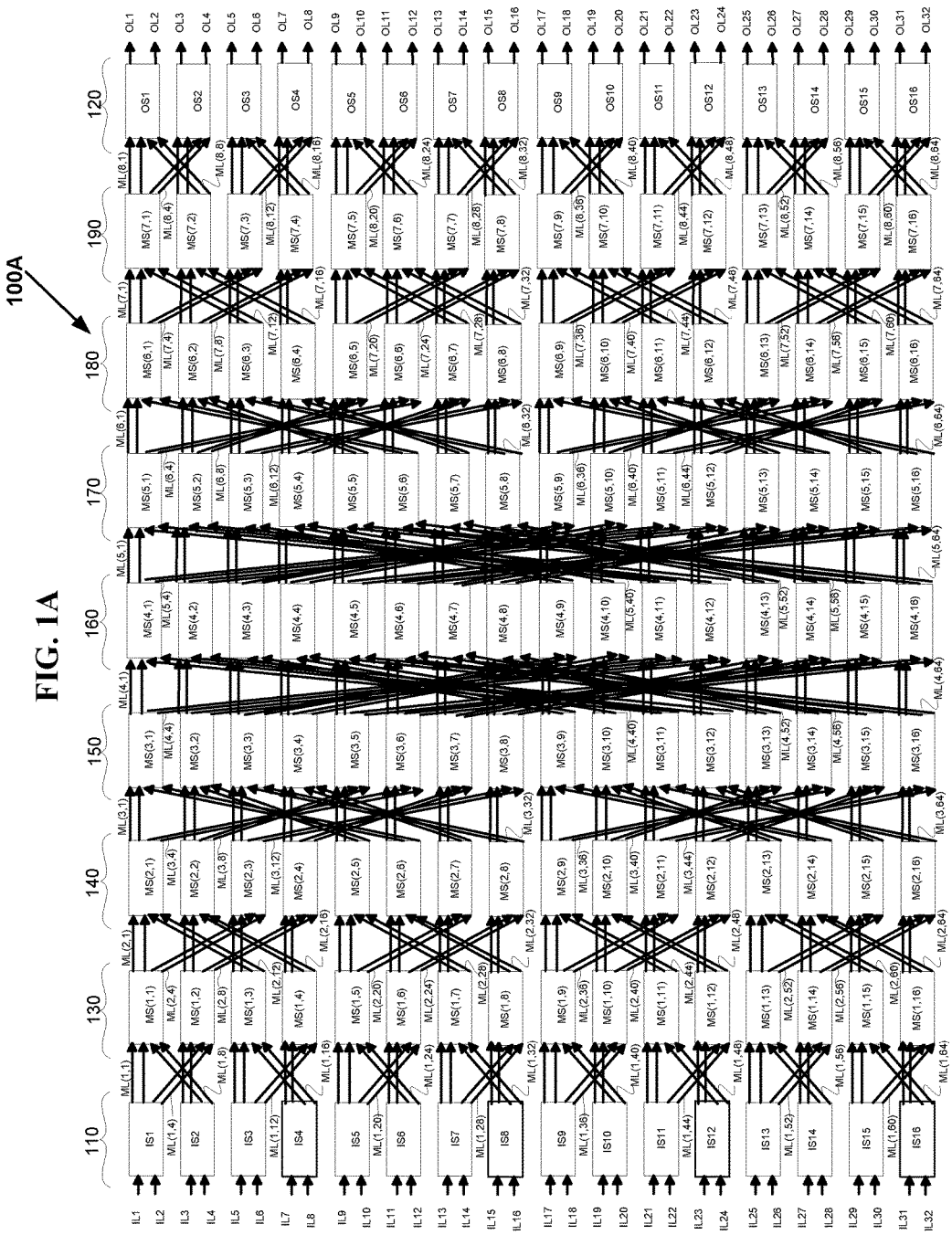

FIG. 1A

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