EXHIBIT 7

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(12) **United States Patent**
Konda

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(54) **OPTIMIZATION OF MULTI-STAGE HIERARCHICAL NETWORKS FOR PRACTICAL ROUTING APPLICATIONS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 107 days.

This patent is subject to a terminal disclaimer.

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(51) **Int. Cl.**
H04L 12/933 (2013.01)
H04L 29/06 (2006.01)

(52) **U.S. Cl.**
CPC ***H04L 49/1515*** (2013.01); ***H04L 29/06081*** (2013.01); ***H04L 49/109*** (2013.01); ***H04L 65/4076*** (2013.01)

(58) **Field of Classification Search**
CPC H04L 49/1515; H04L 65/4076; H04L 29/06081
See application file for complete search history.

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Primary Examiner — Rasheed Gidado

(57) **ABSTRACT**

Significantly optimized multi-stage networks, useful in wide target applications, with VLSI layouts using only horizontal and vertical links to route large scale sub-integrated circuit blocks having inlet and outlet links, and laid out in an integrated circuit device in a two-dimensional grid arrangement of blocks are presented. The optimized multi-stage networks in each block employ several rings of stages of switches with inlet and outlet links of sub-integrated circuit blocks connecting to rings from either left-hand side only, or from right-hand side only, or from both left-hand side and right-hand side; and employ shuffle exchange links where outlet links of cross links from switches in a stage of a ring in one sub-integrated circuit block are connected to either inlet links of switches in the another stage of a ring in the same or another sub-integrated circuit block.

20 Claims, 19 Drawing Sheets

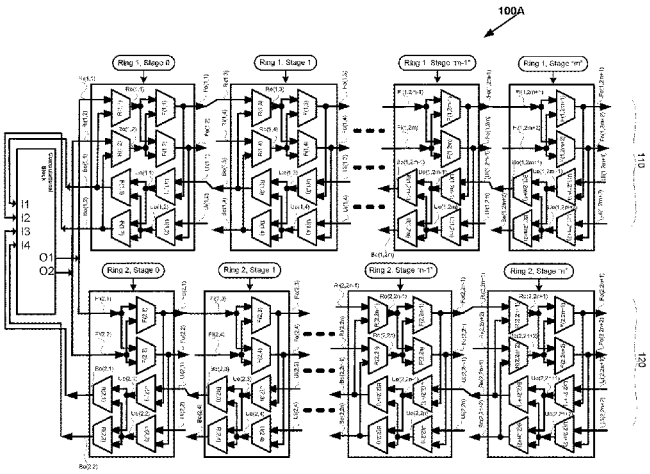

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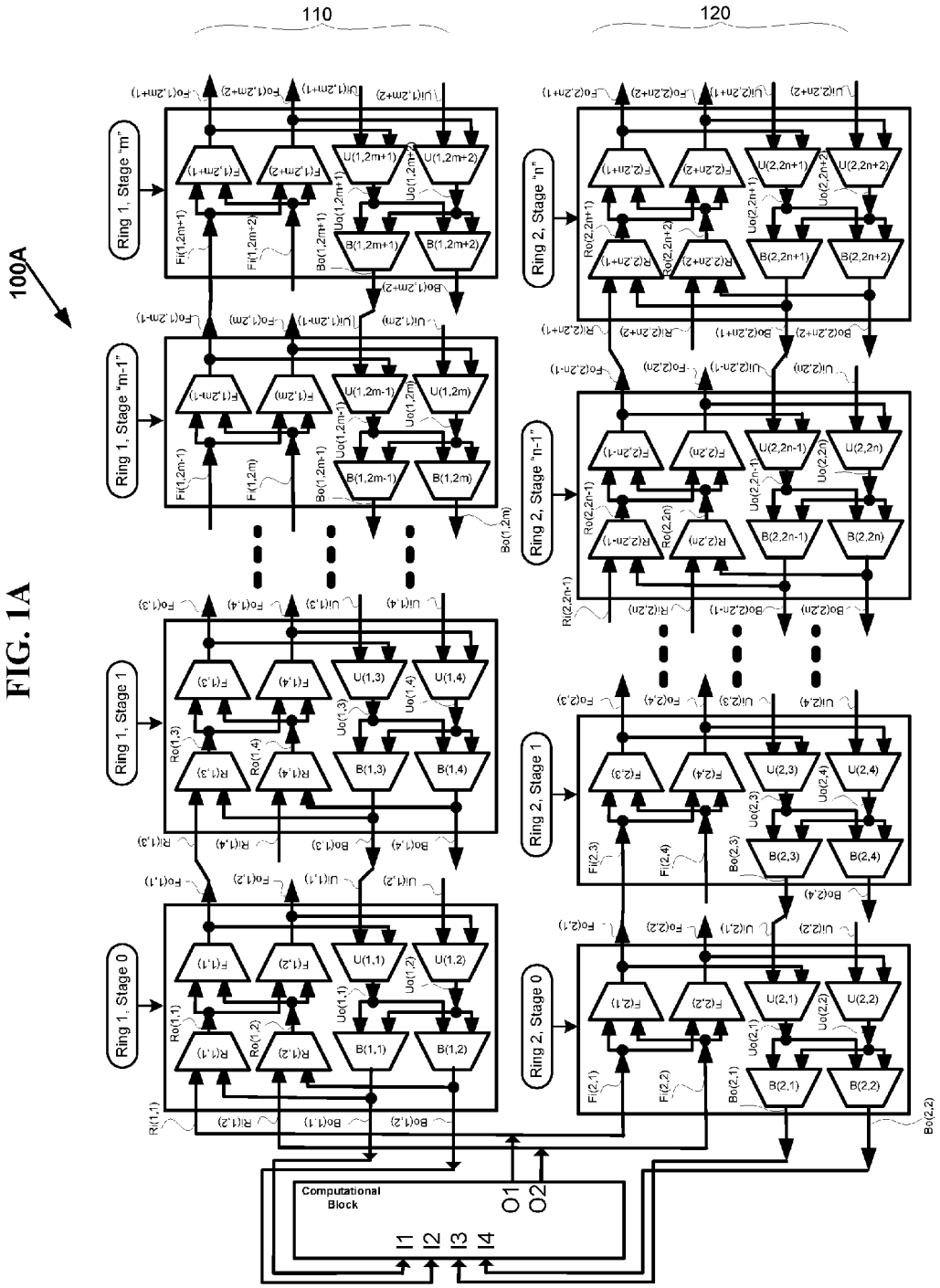
FIG. 1A



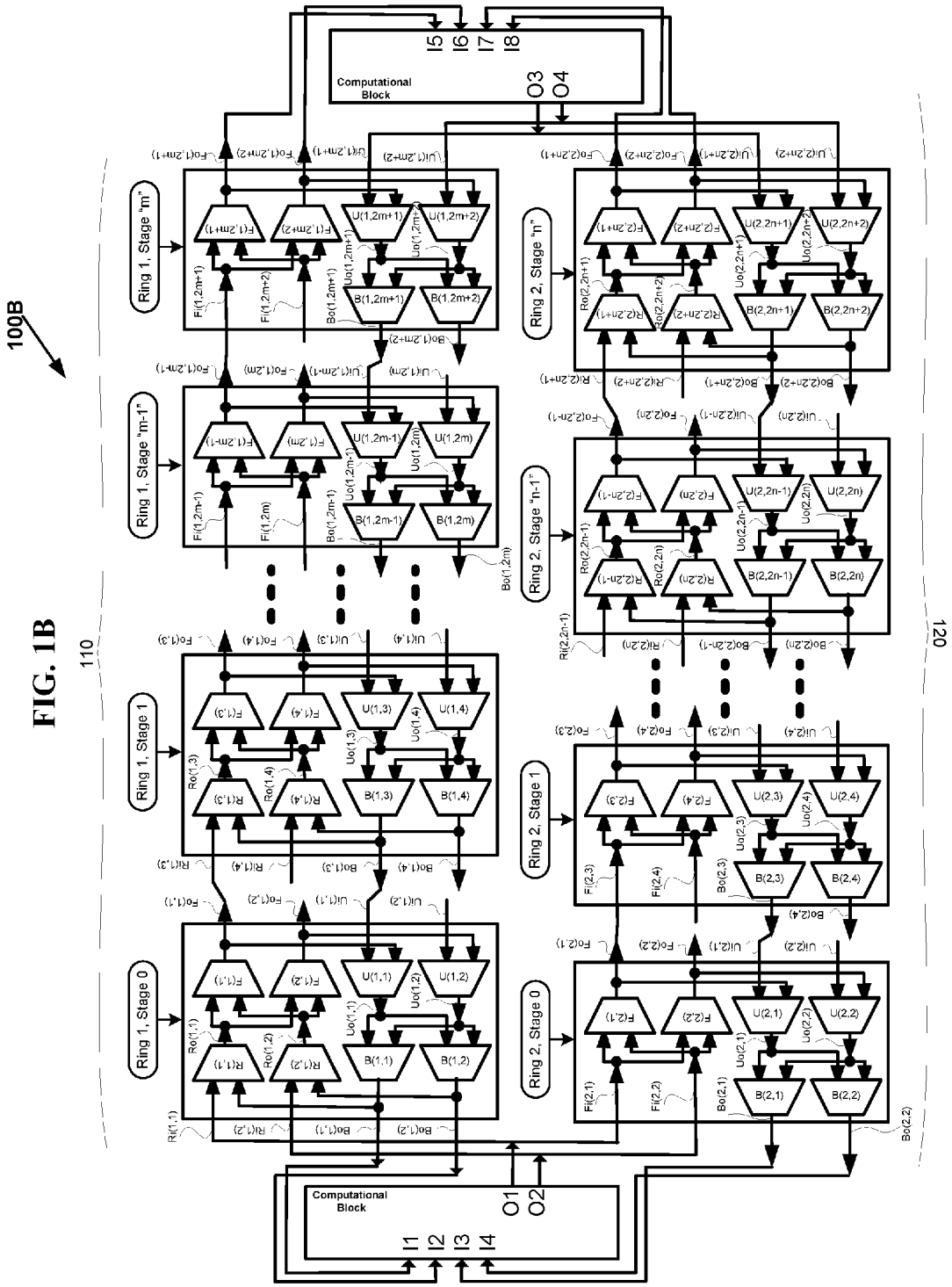


FIG. 1B

DOCKET ALARM

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