

EXHIBIT 4



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Konda

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(54) **VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 183 days.

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Primary Examiner — Vibol Tan

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H03K 19/177 (2006.01)

(52) **U.S. Cl.** **326/41; 326/38**

(58) **Field of Classification Search** **326/38-41; 370/390, 312, 360, 388, 412**
See application file for complete search history.

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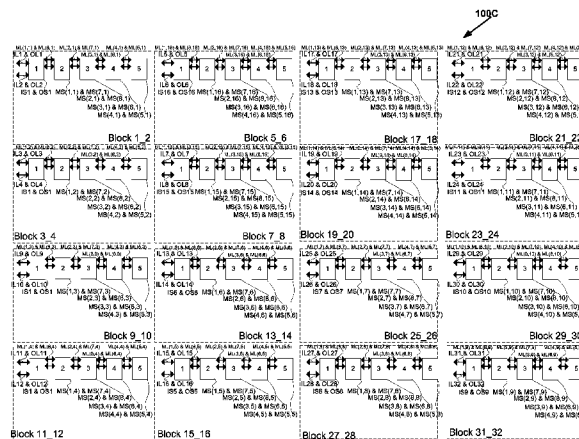
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48 Claims, 39 Drawing Sheets

(57) **ABSTRACT**

In accordance with the invention, VLSI layouts of generalized multi-stage networks for broadcast, unicast and multicast connections are presented using only horizontal and vertical links. The VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa. In one embodiment the sub-integrated circuit blocks are arranged in a hypercube arrangement in a two-dimensional plane. The VLSI layouts exploit the benefits of significantly lower cross points, lower signal latency, lower power and full connectivity with significantly fast compilation.

The VLSI layouts presented are applicable to generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hypercube}(N_1, N_2, d, s)$ for $s=1, 2, 3$ or any number in general. The embodiments of VLSI layouts are useful in wide target applications such as FPGAs, CPLDs, pSoCs, ASIC placement and route tools, networking applications, parallel & distributed computing, and reconfigurable computing.

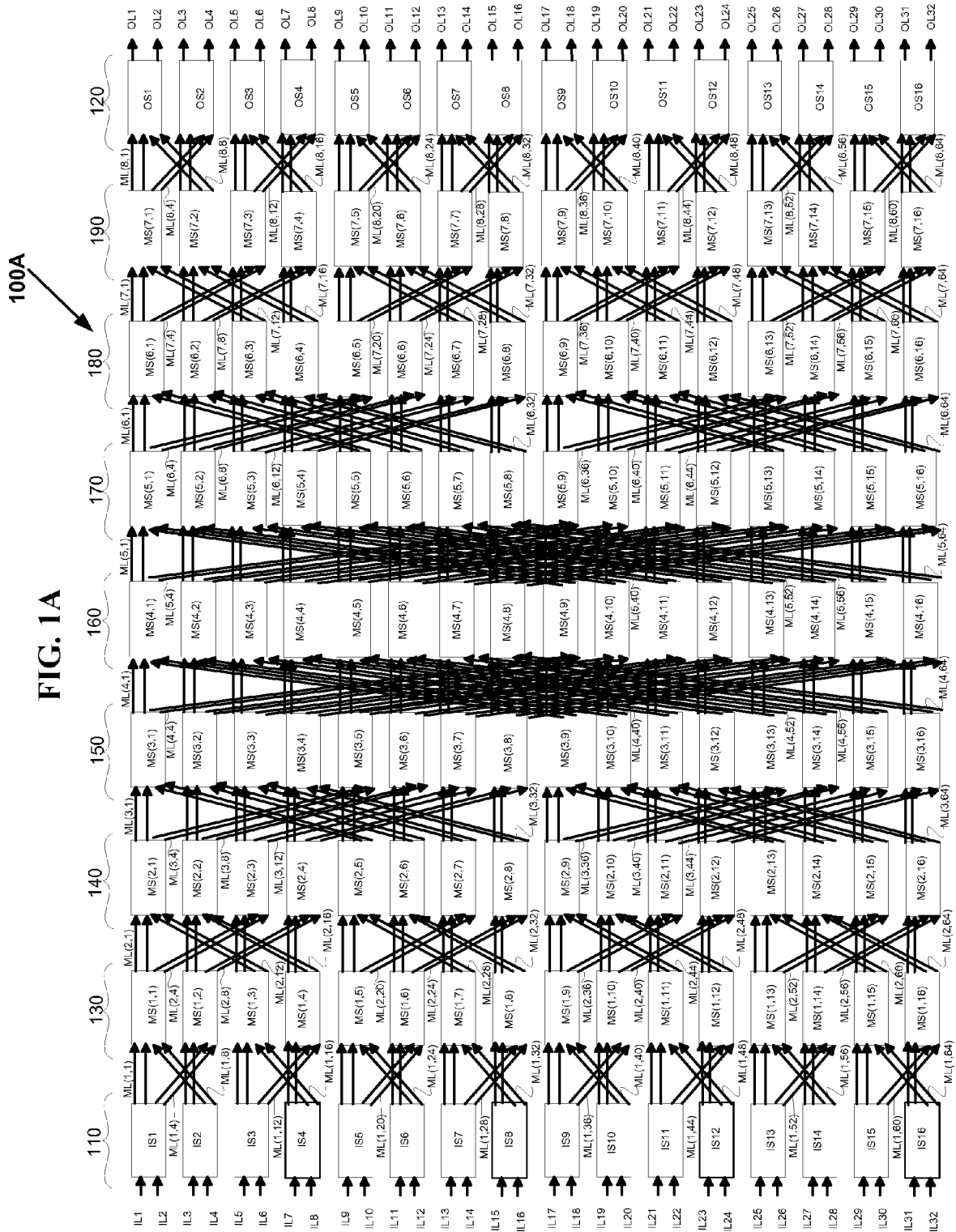


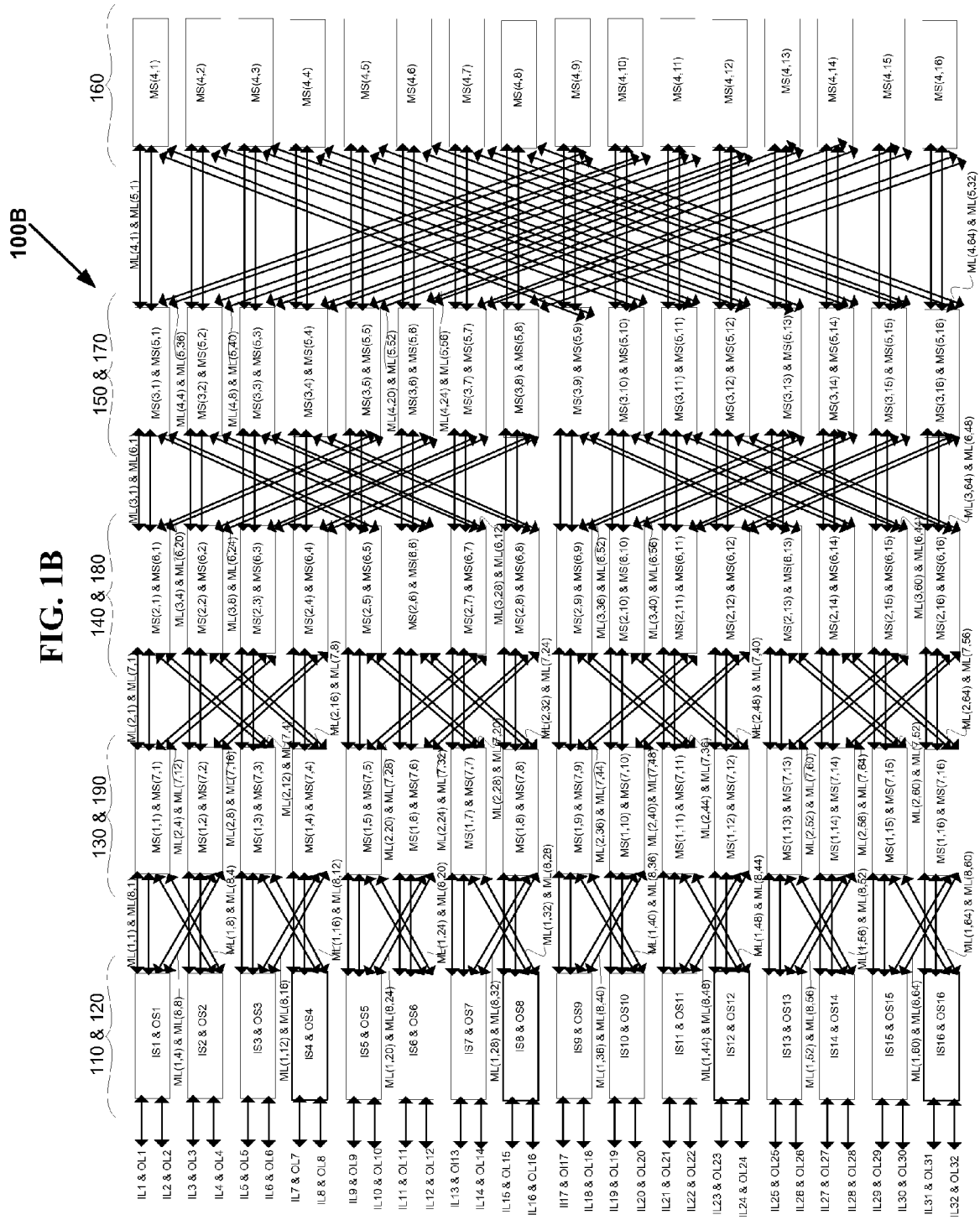
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