

EXHIBIT 2

Volume I
Technical and Management Proposal

Title: Energy-Efficient Butterfly FPGA Hardware and Programming Tools

A proposal submitted to
Dr. William Harrod, DARPA/TCTO
in response to

DARPA-BAA 10-78: Omnipresent High Performance Computing (OHPC)

Technical Area: Energy Efficient Computing

Lead Organization: University of California, Los Angeles (UCLA)
Department of Electrical Engineering
Los Angeles, CA 90095-1594

Type of Business: Other Educational

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Total funds requested: \$2,374,111
Year 1: \$789,927
Year 2: \$792,100
Year 3: \$792,086

UCLA

Date of proposal: August 4, 2010

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August 5, 2010

DARPA/TCTO
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The Regents of the University of California, Los Angeles, is pleased to submit the following proposal in response to solicitation DARPA-BAA-10-78.

Title: "Energy-Efficient Butterfly FPGA Hardware and Programming Tools."

Requested Period of Performance: September 15, 2010 – September 14, 2013

Amount Requested: \$2,374,111

Principal Investigator: Dr. Dejan Markovic
Department of Electrical Engineering
dejan@ee.ucla.edu
310-825-8656

This application is being submitted in contemplation of an agreement containing mutually agreeable terms and conditions applicable to educational institutions conducting unclassified fundamental research.

Since UCLA is a public/State institution, open dissemination of research results and information, commitment to students, accessibility for research purposes, and legal integrity and consistency are part of the University's Principles/Policy. The University does not discriminate and impose restrictions on any individual as a result of their nationalities.

If an award is made, please be advised that if it is funded by budget category 6.3(Advanced Research) and is considered Non-fundamental research, we will not be able to accept the award due to publication restrictions.

Your favorable consideration of this proposal would be appreciated. Technical questions should be directed to Dr. Markovic. Administrative and contractual questions, should be directed to me at (310) 794-0155 or via email at jzhu@research.ucla.edu.

Sincerely,

A handwritten signature in black ink that reads 'Julia Zhu'.

Julia Zhu
Senior Grant Analyst

Table of Contents

Executive Summary	3
Section II – Technical Details	5
2.1. PowerPoint Summary Chart	5
2.2. Innovative Claims for the Proposed Research	6
Problem Description	6
Research Goals	6
Expected Impact	7
2.3. Proposal Roadmap	8
2.4. Technical Approach	10
2.4.1. Network Architecture and Routing Tools	14
2.4.2. Hardware Design	15
2.4.3. Hardware Mapping	19
Demonstrations and Technology Transition	22
2.5. Statement of Work	24
2.6. Intellectual Property	26
2.7. Management Plan	28
2.8. Schedule and Milestones	30
2.8.1. Schedule Graphic	30
2.8.2. Detailed Task Description	31
2.8.3. Project Management and Interaction Plan	33
2.9. Personnel, Qualifications, and Commitments	34
2.10. Organizational Conflict of Interest Affirmations and Disclosure	36
2.11. Human Use	39
2.12. Animal Use	38
2.13. Statement of Unique Capability Provided by Government or Government-Funded Team Member	39
2.14. Government or Government-funded Team Member Eligibility	40
2.15. Facilities	41
References	42
BEEcube Support Letter	43

Executive Summary

UCLA offers to perform research on a revolutionary new FPGA technology consisting of FPGA hardware and supporting mapping tools. We will design, fabricate, and test hierarchical FPGA interconnect network to demonstrate FPGA technology that is 15x more energy-efficient than existing FPGAs. The new interconnect architecture allows for significant reduction in the number of switch points, buffers, and wire length in comparison to standard 2D-mesh architecture used by existing FPGAs. The proposed technology is a radical departure from 2D-mesh design, which for N logic blocks has complexity $O(N^2)$, incomplete and heuristic routing. The proposed technology has only $O(N \cdot \log_2 N)$ complexity, complete and fully deterministic routing. The proposed technology has significant benefits: 15x lower power, 3x lower area, 2x higher performance compared to existing FPGA technology. The new FPGA technology will be used to demonstrate HPC benchmarks with a 15x higher power efficiency for DOD and commercial users. The PI has established interactions with industrial partners that will lead to the transition of ideas into the commercial space.

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