

# EXHIBIT 13

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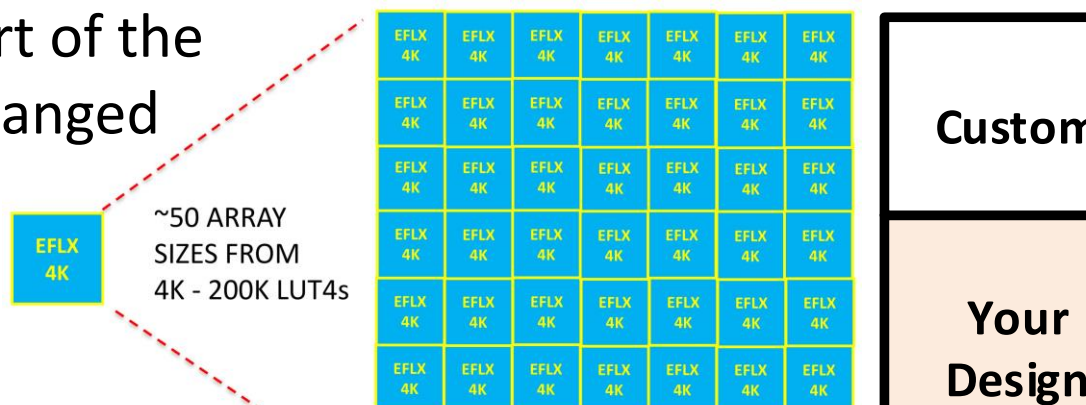
# Virtual Array Architecture for eF

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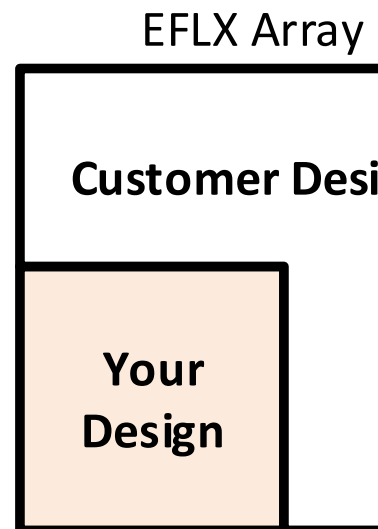
# Why the Need for Virtual Arrays

- Security:
  - Keep your “secret sauce” design masked from the customer
- Preserve Performance & Density:
  - “Harden” your optimized design for best performance & density on EFLX arrays, even when the rest of the design changes
- Runtime:
  - Avoid performing P&R on the entire array when your part of the design is unchanged



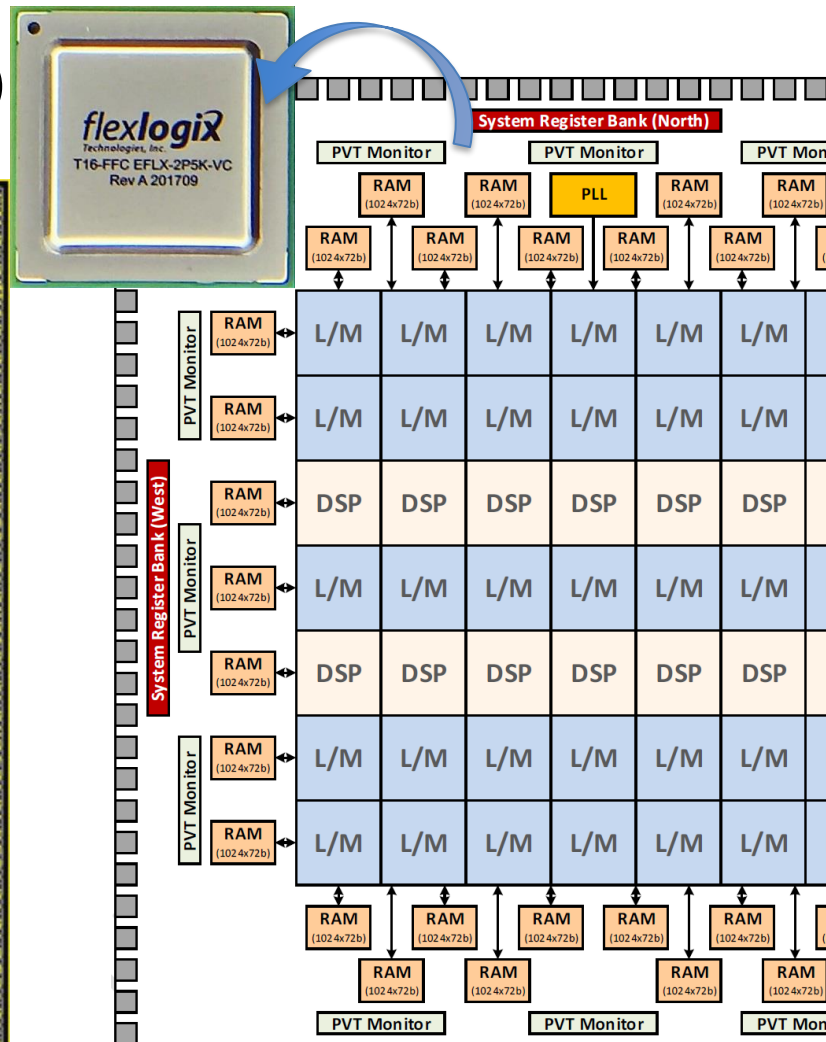
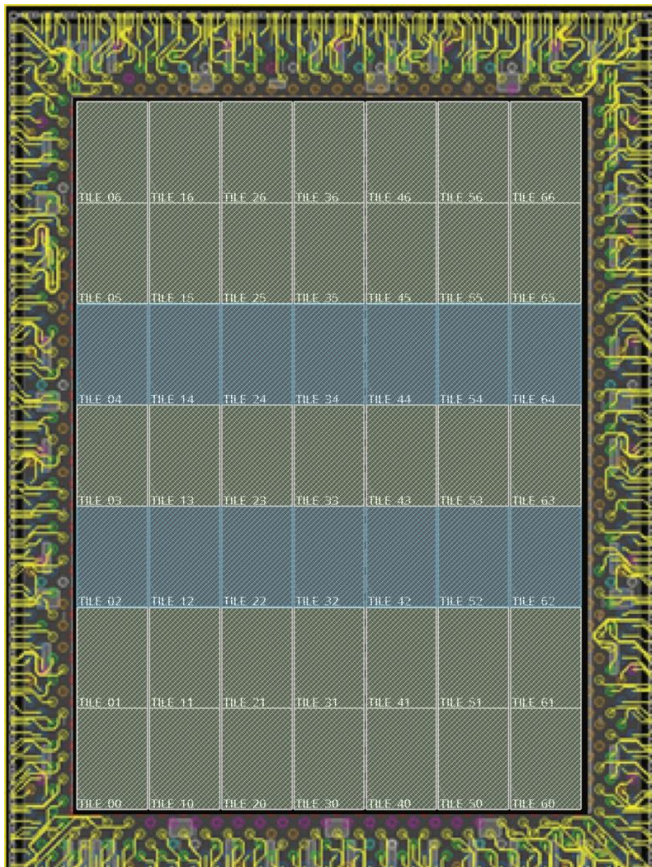
## Virtual Array Solution

- Have your “secret sauce” IP and customer design on one EFLX array
  - Designs inside black-box tiles are not visible by end-user
  - Remaining EFLX tiles remain user-programmable
- Maintain optimal performance and density of EFLX
  - Preserve P&R performance in black-box tiles
  - Black-box bitstream is merged directly into the final bitstream
- Improve EFLX Compiler runtime
  - Designs in black-box tiles are not P&R’ed again



# Example: EFLX200K Test Chip in TSMC1

- 7x7 Array
  - 114,240 6-LUTs (~183K LUT4s)
  - 560 22x22 MACs



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