EXHIBIT 10

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flexlogix Technologies, Inc.

eFPGA IP Density, Portability & Scalability

There are multiple eFPGA suppliers in the market today: Achronix, Adicsys, Efinix, Flex Logix™, Menta, QuickLogic.

There are 3 different business models and engineering approaches to eFPGA which you should understand to assess how it will impact your success in using their eFPGA IP and their viability as a supplier long term.

	Type of eFPGA company	**FPGA Chip Companies Offering eFPGA**	**Soft-IP Companies**	**Flex Logix**
Design Approach	**Interconnect**	Mesh	Mesh	Mixed Radix Hierarchical-Mesh
	LUT Size	4-input-LUT	Variable?	6-input-LUT
	Design	Full-custom Hard IP	RTL IP or Standard Cell Hard IP	Standard Cell Hard IP
	Different sizes	Modular custom construction	Software generator?	Tiling with no GDS change
	Validation Chip	None made public	None made public	Proves each eFPGA IP core in silicon and validates over temperature/voltage
Implications	**Relative Density (1x is highest)**	1x	0.3-0.5x	1x
	Metal Stack	GDS changes: must re-route, if possible, for each metal stack	?	Compatible with almost all metal stacks with no GDS change
	Different Sizes	GDS changes; smallest size unknown; up to 1M LUTs	GDS changes; <10K LUTs	No GDS change; 100 to 200K LUTs with roadmap to 800K LUTs
	GDS Delivery in your process, metal stack, size	Longest if any modifications required	Fast	Fast
	Risk	Significant GDS changes for every metal stack/process variation/array size	Not every array size is validated	GDS is proven in silicon and works across almost all metal stacks, process variations and array sizes

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FPGA Chip Companies Providing eFPGA IP

FPGA chip companies generally build a new generation of FPGAs every ~3 years when there is a major advance in process technology.

They pick one foundry, one node, one variation of that node and do full-custom circuit design with typically the maximum or near-maximum number of metal layers in order to get the highest density FPGA they can. It takes them most of the 3 years to do the complex engineering required.

Since FPGA customers want a range of sizes and some variation in the ratio of options like DSP/RAM, the FPGA chip companies will construct their FPGAs from some modular pieces: a block of LUTs, a DSP block, and typically a block-RAM (dual port). The 3-10 different sizes of the FPGA are put together from the blocks with circuit designers tuning the mesh interconnects and I/O's for the array size.

Their business model is to optimize to make the best FPGAs. What happens when they provide embedded FPGA IP?

1st There are typically dozens of metal stacks that a foundry supports. The bottom 4-7 layers, depending on the process, are generally common because of foundation IP like standard cells and memories. Above that, some customers want fewer layers for lower cost for simpler circuits; others want maximum layers for large, complex circuits. There are many variations of thicknesses/widths by layer to optimize for each customers design. FPGA companies usually design their chip with maximum or near-maximum metal layers which significantly limits the supported metal stacks to one or two. If a customer wants a different metal stack, they have to re-route. If the customer wants the same number of metal layers but with variations in thickness for some of the layers, timing will have to be redone and likely re-routing of the whole design along with circuit changes to offset timing/DRC issues with thicker/thinner metal. If the customer wants fewer metal layers, it may be impossible: presumably the FPGA chip uses the number of layers it does because it was not possible to route with fewer layers. The time to do all this work is likely 4-6 months with significant engineering expense.

2nd Foundries continually improve each of their process nodes for yields, fewer metal layers and shrinks with a new variation every year or so. Since FPGA chip companies do full-custom design, they will need to re-simulate and likely re-design multiple portions of their chip to support the incremental changes to the process. (Whereas standard cells are generally useable across 2 or 3 incremental variations because they use less aggressive logic design rules AND the

foundries try to keep the standard cells the same for their customers to migrate easily to the newer process variation).

3rd Supporting a range of array sizes and options (DSP, RAM) requires custom engineering: the blocks may be modular, but the connections between them and most importantly the interconnect will need to be redone especially since the amount of interconnects grows with N^2 for mesh interconnect designs. And the I/O ring is custom for each different array size.

4th Since the GDS changes for every metal stack and array size and process variation, it is uneconomical to do a validation chip for every GDS change.

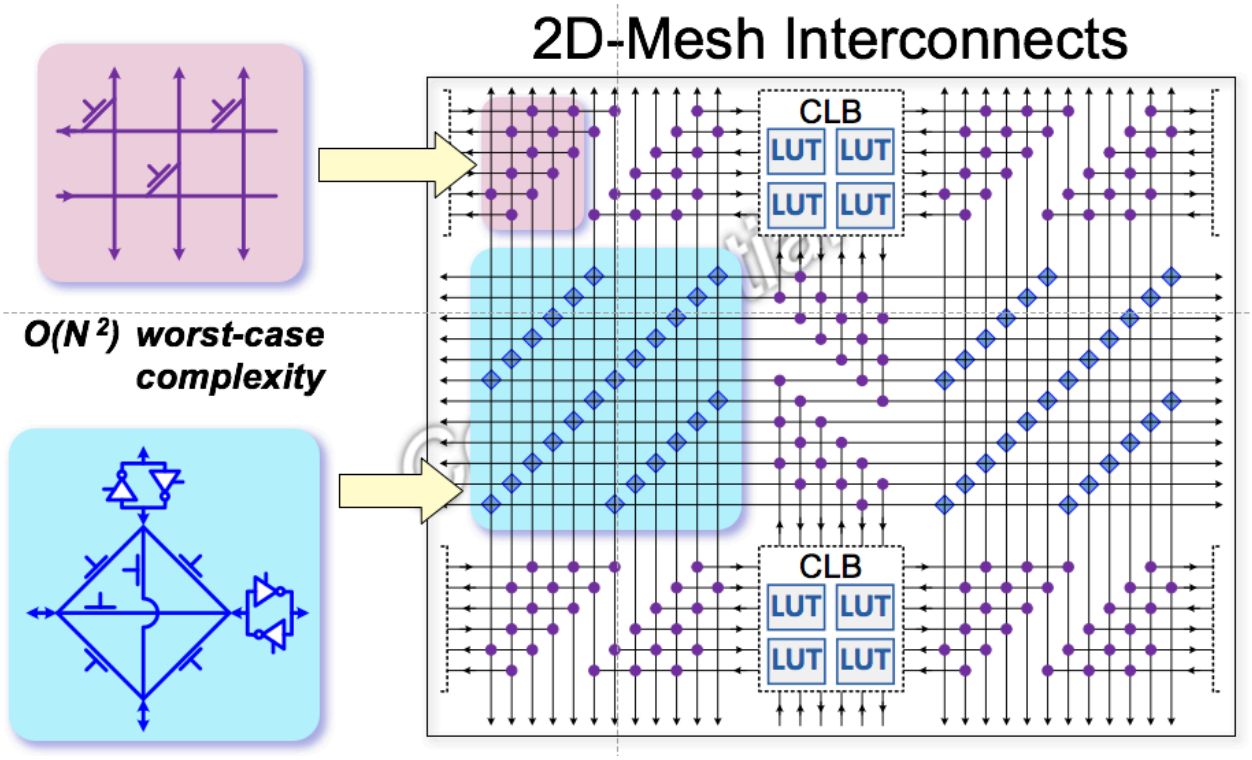

Figure 1: Traditional 2D-Mesh Interconnect diagram illustrates the non-uniformity of a mesh network across the FPGA. Any change to the area or configuration will require re-implementing the interconnect, effectively creating a new embedded FPGA implementation.

The FPGA chip companies have been in business >10 years but offer eFPGA on only a few nodes.

The engineering investment to support different array sizes and options and metal stacks within an existing node/variation are significant; the engineering investment to port a full-custom design to a new node are much greater (that's why FPGA companies usually only do a generation every few years).

This is probably why the big FPGA chip companies don't bother with eFPGA: it is a costly distraction to their primary business with, for them, a low return on investment.

Pure eFPGA IP Companies: Soft IP

eFPGA soft IP companies offer a software tool that will generate RTL for an array based on inputs such as array size, I/O count, etc. The customer can then use EDA tools with a standard cell library to implement the eFPGA in any process – but the density is very low: FPGAs are very regular and benefit from structured placement. This approach has some use in test chips or very low volume products such as aerospace/defense.

One of these companies now offers hard IP on a couple of foundries/nodes. For that company, their maximum array size is <<10K and there are only a handful of sizes/option combinations to choose from. Density for the smallest arrays is ~0.5x of a full-custom FPGA; and for the largest arrays ~1/3 of a full-custom FPGA. Presumably what is happening is the N^2 complexity growth in interconnect for larger arrays. Their largest array is 2x the LUTs and Flip-Flops of their mid-size array, but is ~3x the silicon area! This trend in interconnect complexity growth is probably why there are no large arrays offered. The number of metal layers required or the range of metal stacks they are compatible with is not public.

Each array size is a different design so a validation chip for one does not prove the others. Doing a validation chip for each array size is uneconomical.

Pure eFPGA Hard IP: Flex Logix

Flex Logix is the youngest of the companies providing eFPGA but offers eFPGA on more process nodes/variations (7 foundry and 1 captive) and over a wider range of sizes than any competitor.

We started the company based on Cheng Wang's revolutionary interconnect which he developed working with others at UCLA while doing 5 different FPGA test chips of increasing complexity over multiple process nodes prior to starting Flex Logix.

In traditional FPGAs, the FPGA fabric is 70-80% interconnect and only 20-30% of the area is logic/LUTs.

Cheng's test chips were limited in size by budget suppliers: To get more logic on the chip he came up with a new interconnect that was much denser than the traditional mesh. And its' complexity grows more slowly than mesh for larger array sizes.

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