EXHIBIT 1

1. Identification and Significance of the Problem or Opportunity

1.1 Objective: In this project, we plan to prepare a Phase I feasibility study of integrated circuit micro-cells based on regular geometry for use in our proprietary **hierarchical FPGA interconnect architecture**. The objective of the overall 3-phase FPGA project is to substantially reduce energy and cost of low-volume digital signal processing by using hierarchically routed interconnect, **regular-geometry micro-cells**, and associated tool-flow for routing and hardware mapping. Figure 1 illustrates our overall vision for the project. While the FPGA architecture and associated tool-flow for design and algorithm mapping reduces cost in design time and chip metrics (the focus of Phases II and III), enforcing regular layout geometries at the cell level provides additional reduction in the manufacturing cost, particularly in advanced technology nodes such as 32nm and below. This proposal will thus evaluate the design of regular layout cells for FPGA design and compare their circuit and cost metrics to standard-cell based CMOS design. Our team is formed from an industrial innovator (Dr. Venkat Konda) who has strong patent portfolio in routing networks (Phase II work), and academic leaders in the areas of regular geometry circuit design (Prof. Puneet Gupta), and energy-efficient architecture design and associated tool-flows (Prof. Dejan Markovic). Our objective is to develop **low-cost digital signal processing hardware and tool-flows** for emerging markets such as wireless and sensor applications where cost and power consumption are key concerns.

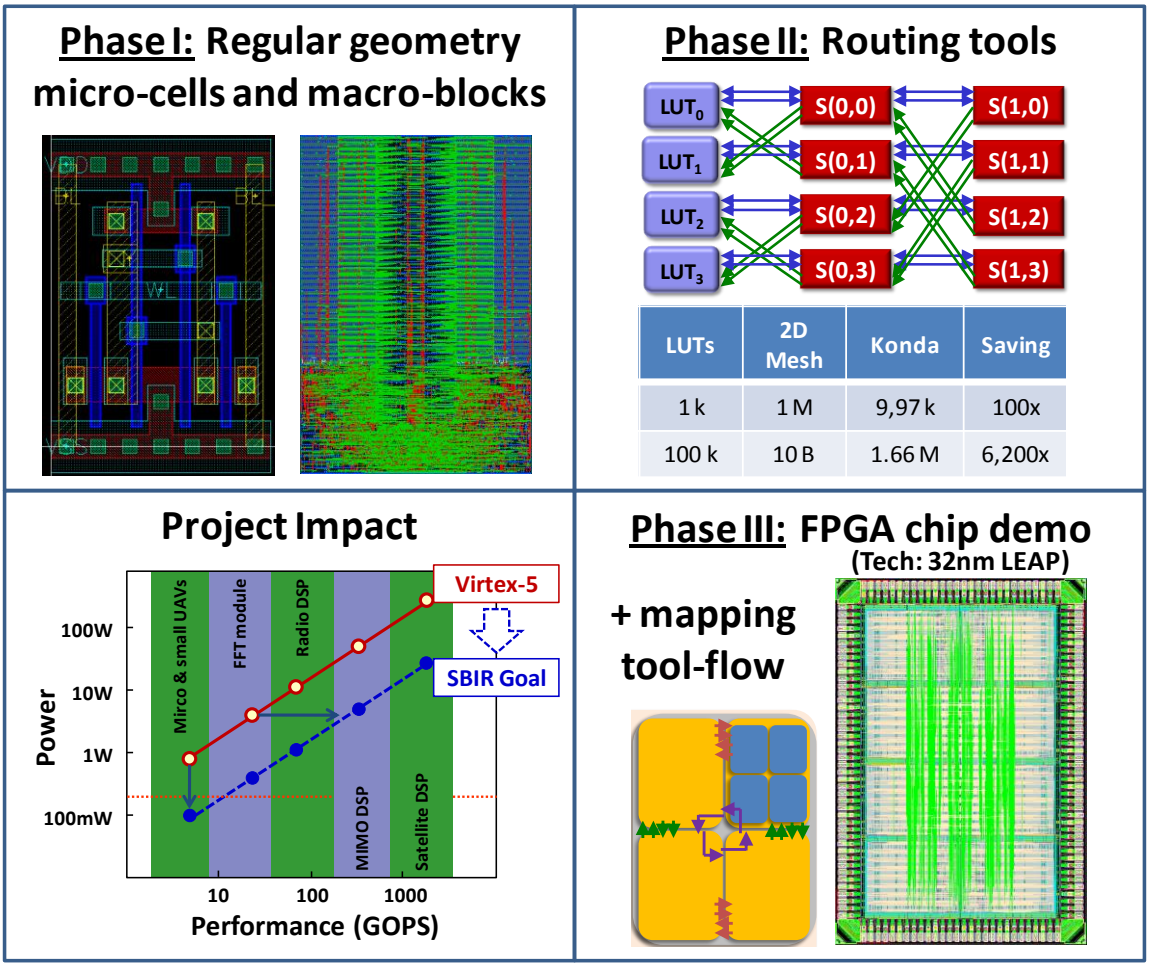

Figure 1: Regular-fabric micro-cells and blocks (output of Phase I) will be used to route Konda's hierarchical interconnect architecture (output of Phase II) and further integrated on a demo FPGA chip with supporting mapping tool-flow (output of Phase III) to demonstrate significant improvements in chip size, performance, power, and also manufacturing cost.

1.2 Problem Addressed: With increasing cost of semiconductor design and manufacturing, enforcing regularity at all layers from device technology to hardware architecture is essential for future low-power and low-cost digital signal processing hardware. At the architecture level, FPGA-like regularity is becoming an attractive solution particularly for low-volume applications, but the adoption of FPGAs will be greatly challenged with their excess power, area, and performance due to the massive FPGA interconnect. The complexity of the FPGA interconnect is a quadratic function, $O(N^2)$, of the number of processing elements, N. To mitigate the interconnect challenge, we will make use of hierarchically routed and proprietary Konda interconnect architecture which has greatly reduced complexity, $O(N \cdot \log_2 N)$, which results in improved area, power, and performance of FPGA chips. Additionally, we must face unique challenges of scaled technology and enforce regularity in the layout cells (micro-cells). With the slow development of Extreme Ultra Violet (EUV) lithography, double patterning technology (DPT) appears as the most viable lithography solution for 32nm and later technology nodes [1]. DPT allows for more compact and better-yielding layout using mask decomposition to effectively increase pitch size. To find best DPT decompositions as applicable to FPGA micro-cells and building blocks, we propose to investigate micro-cell routing algorithms and characterize the cells in energy-area-performance space as compared to their standard-cell based CMOS counterparts.

1.3 Proposed Solution: Our approach will consist of:

(a) Research the state-of-the-art regular layout geometries and routing algorithms for micro-cells,
(b) Innovate and provide unique solutions to overcome challenges at the cell layout, circuit, and architecture levels,
(c) Develop modeling and simulation framework that will guide the final selection of regular-geometry micro-cells to be used in FPGA macro-blocks such as lookup tables (LUTs), DSP slices, block RAM (BRAM) modules, switch matrix (SM) elements that include switch boxes (SBs) and configuration memory, and
(d) Perform **energy, area, performance, yield, and variability evaluation** of the propose micro-cell and macro-block structures for use in hierarchical FPGA interconnect architecture.

As a quantitative measure of our Phase I study, we plan to provide an extensive list of circuit metrics as listed in Table 1. The metrics include area, energy, performance, variability, and yield estimates for standard-cell and proposed regular-geometry cells (both at the micro and macro levels). The outcome of Phase I will be to populate Table 1 with quantitative measures of functional-block metrics, and to provide associated solutions for layout cells. The layout cells from Phase I will be subsequently used in hierarchical FPGA interconnect architecture (Phase II), FPGA chip and hardware mapping tool-flow (Phase III) to provide over 10x improvement in power compared to the state-of-the-art FPGAs.

Table I: Feasibility study of quantitative figures of merit of layout cells for FPGA application.

Metric / Functional Block	Energy (fJ)		Delay (ps)		Variability (%)		Yield (%)	
	Std-cell	Regular geometry	Std-cell	Regular geometry	Std-cell	Regular geometry	Std-cell	Regular geometry
NAND gate								
Flip-flop								
AOI gate								
Full adder								
4-input LUT								
DSP slice								
Switch box								
Switch matrix								

1.4 Proposal Strength: The main strength of the proposed work is the multi-disciplinary approach that spans technology, circuits, architectures, and algorithms for exploiting regularity multiple hierarchical layers in the design of digital signal processing hardware. The combined effort in the aforementioned areas will lead to the development of low-cost FPGA platform based on regular-geometry layout cells, hierarchically routed interconnect architecture, and tool-flow for area-efficient hardware mapping of digital signal processing algorithms. Our strength in all aspects from layout to algorithms will allow for (a) layout cell development, (b) accurate development of device and circuit specifications, (c) allow for extensive analysis to predict yield, power consumption, chip area, and performance, (d) provide full hardware/software demonstration at the end of the 3-phase program. Furthermore, our team has extensive experience in energy-efficient integrated circuits and architectures, CAD algorithms and layout cells, as well as network architectures and supporting routing algorithms.

1.5 Market Opportunity: We see a great market potential in broad area of digital signal processing hardware where the cost and power consumption are key challenges. Our final goal is to develop a simple and low-cost FPGA hardware/software technology based on regular layout cells, regular hierarchical interconnect architecture, and tools for block routing and hardware mapping. The potential markets include both commercial and defense segments. With greatly reduced power consumption and cost, the technology will particularly impact energy-starved applications such as embedded electronics and distributed sensors. The technology will also provide a solution to rapid prototyping and emulation for a variety of communications and imaging applications. To reduce design cost and ensure **scalability**, our approach will deliver **hierarchical methodology** from micro-cell layout to final chip architecture and supporting tool-flows.

1.6 Company Profile: Konda Technologies, Inc. is a startup company based in San Jose, CA. The company was founded in 2007 to develop & commercialize interconnect IP applicable for various products including FPGA routing interconnect, System-on-Chip interconnects and warehouse-scale datacenter switch networks. Our main customer today is Tier Logic Inc, a 3D-FPGA startup. The company has been engaged with vendors such as Xilinx Corporation, Altera Corporation and Cisco Systems.

2. Phase I Technical Objectives

2.1 Objective 1: Development of reusable infrastructure of regularity evaluation at cell-level
We will develop a tool infrastructure to allow for evaluation and exploration of regular layout styles. This would include fast estimation-based methods as well as layout generation and simulation based methods.

2.2 Objective 2: Analysis of regularity tradeoffs at different layers and identification of layout styles suitable for the FPGA architecture
Using the regularity evaluation framework developed above, we will identify the optimal choice of regular layout styles on front-end layers (poly, active, M1, M2, contact). This will be applied to varying levels of design complexity ranging from standard cells to entire FPGA functional macros.

2.3 Objective 3: Develop a comprehensive plan for Phase II
The outcome of Phase I will be a comprehensive study of micro-cells and macro-blocks that will be used in Phase II to implement hierarchical interconnect architecture. The objective is to significantly improve energy, area, and performance of the FPGA hardware. The output of Phase I will be guided by the metrics outlined in Table 1. Phase I solutions will be developed with tight interaction between architecture, circuit, and process parameters to ensure globally optimal solutions. We will propose an IP library and associated tools to reduce design cost and facilitate commercial adoption of our technology.

3. Phase I Work Plan

3.1 Introduction and Prior Art

Generally, regularity makes patterning easier. Inserting dummy features to ensure uniform density or to "isolate" standard cells from surroundings has been commonly followed approach. For more regularity, set of layout constraints or restrictive design rules [2], can be enforced to guarantee a lithography-friendly regular layout. As an example, a unidirectional fixed-pitch poly layer is enforced in Intel's 45nm process. Because of the success of such gridded design rules in enhancing printability and reducing variations [4], such rules might be adopted to pattern other patterning layers such as metal and contacts/vias. This principle of restricting the layout is pushed to the extreme in [5] where layout is constructed out of pre-characterized regular fabrics (as opposed to design rules). A regular layout approach can be excessively conservative especially for layouts where patterning imperfections would otherwise be tolerable [2]. Nevertheless, increasing degree of regularity is expected to make patterning even feasible in the near term.

Another important point is that regularity need not imply 1D gratings. The basic "template" for regularity could be something else while still ensuring good, low-cost printability (e.g., see [6]). The template printability can be optimized, for example, using source-mask optimization (SMO) or using character projection in maskless E-beam direct-write. Part of our work will also investigate if regularity other than gratings can be useful.

3.2 Our Approach

Our approach within this proposal, and in line with the SBIR call, is to examine routing tools for regular-geometry layout cells. The goal in Phase I will be to develop routing tools and layout cells for FPGA building blocks. The layout cells will vary in granularity from simple logic gates to complex blocks such as look-up tables, logic slices, switch boxes, and memory components. The regular cells will be characterized for density (area), yield, energy, and performance and compared to regular standard-cell based approach. The regular cells will be used in Phase II for interconnect architecture routing. The cells and routing tools will be made available as IP to facilitate rapid commercialization.

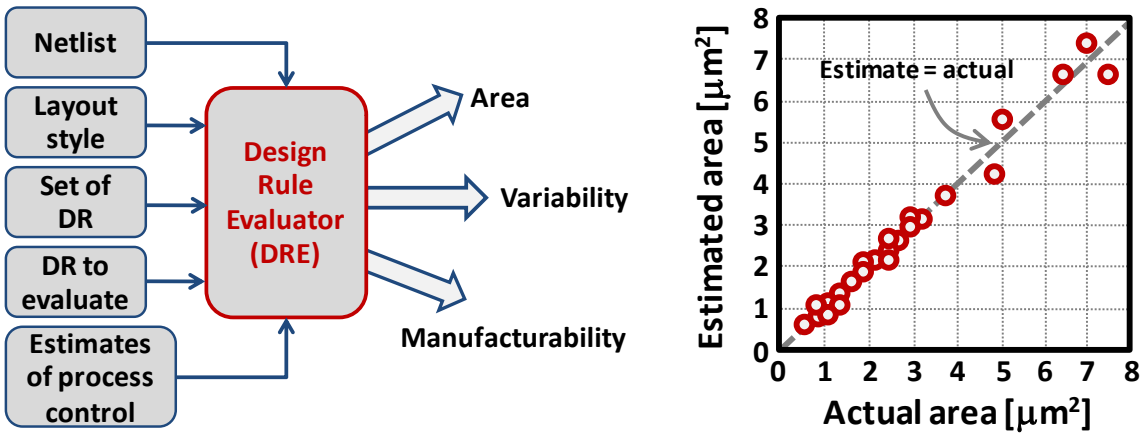

Figure 2: Regularity evaluation framework (left), DRE results on 45nm Nangate open-cell library (right).

Regularity is a continuum of possibilities and it has significant impact on area, delay, power as well as expected manufacturing yield. It therefore is very important to co-optimize design rules, regular layout styles as well as cell architectures. We have developed a Design Rule Evaluator (DRE) framework (see **Error! Reference source not found.**) which predicts the impact of layout style and design rule changes on important circuit metrics for standard cells as well as small custom blocks. DRE can run through a 100+ cell 45nm cell library in a few minutes with less than 2% average estimation error (see **Error! Reference source not found.**) making it perfectly suited for design space exploration of layout

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