Exhibit J

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Paper No. 24
Date Entered: June 1, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
and
QUALCOMM INCORPORATED, GLOBALFOUNDRIES INC., GLOBALFOUNDRIES U.S. INC., GLOBALFOUNDRIES DRESDEN MODULE ONE LLC & CO. KG, GLOBALFOUNDRIES DRESDEN MODULE TWO LLC & CO. KG,
Petitioners

v.

DSS TECHNOLOGY MANAGEMENT, INC.,
Patent Owner

Case IPR2016-00290[1]
Patent 5,965,924

Before BRYAN F. MOORE, BRIAN J. McNAMARA, and MINN CHUNG, *Administrative Patent Judges*.

McNAMARA, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and
37 C.F.R. § 42.73

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[1] Case IPR2016-01312 has been joined with this proceeding.

BACKGROUND

On June 8, 2016 we instituted an *inter partes* review of claims 7–12, 15, and 17 of U. S. Patent No. 5,965,924 ("the '924 Patent") based on a Petition filed by Intel Corporation. Paper 10 ("Dec. to Inst."). DSS Technology Management, Inc. ("Patent Owner") waived its right to file a Preliminary Response. On August 29, 2016 we instituted *inter* partes review of the same claims on the same grounds based on a substantially identical petition filed by Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, Globalfoundries Dresden Module Two LLC & Co. KG, in IPR2016-01312. We then joined IPR2016-00290 and IPR2016-01312. Papers 17, 18. In this joined proceeding, we refer to Intel Corporation, Qualcomm Incorporated, Globalfoundries Inc., Globalfoundries U.S. Inc., Globalfoundries Dresden Module One LLC & Co. KG, Globalfoundries Dresden Module Two LLC & Co. KG, collectively as "Petitioner."

On September 7, 2016, Patent Owner filed a Patent Owner Response that contained no citations to evidence and no argument, other than noting that in contrast to the standard applied in reaching a decision to institute (i.e., a reasonable likelihood Petitioner will prevail on its challenge to patentability of a claim), the standard for reaching a final decision is whether the Petitioner proved unpatentability by a preponderance of the evidence. PO Resp. 2. Patent Owner then stated it "defers to the Board to make this determination based on its impartial analysis of the prior art and Petitioners' arguments." *Id.*

In its Reply filed on December 7, 2016, Petitioner stated that Patent Owner has provided no testimony or any other evidence that contradicts or

rebuts the testimony of Petitioner's expert, Dr. John Bravman, and that the challenged claims should be found unpatentable (Paper 21, "Pet. Reply").

We did not conduct an oral hearing in this case.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is issued pursuant to 35 U.S.C. §318(a). We base our decision on the preponderance of the evidence. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

Having reviewed the papers submitted by the parties and the supporting evidence, we conclude that Petitioner has demonstrated by a preponderance of the evidence that the challenged claims are unpatentable.

THE '924 PATENT (Ex. 1001)

The '924 Patent relates to semiconductor fabrication in general, and in particular concerns a metal plug local interconnect that is formed in the same process of forming metal plugs that are already designed as sub-metal plugged contacts. Ex. 1001, col. 1, ll. 9–11. The '924 Patent discloses that in semiconductor fabrication, it is often necessary to make a local interconnect between a gate polysilicon layer to N+ or P+ diffusion regions. *Id.* at col. 1, ll. 16–17. According to the '924 Patent, conventionally such local interconnects were fabricated using buried contacts, as shown in Figures 1A and 1B of the '924 Patent (*id*. at col. 1, l. 25–col. 2, l. 11) or with a metallic local interconnect strap to shunt from a gate polysilicon to a diffusion region, as illustrated in Figures 2A and 2B of the '924 Patent (*id.* at col. 2, l. 12–41).

The '924 Patent discloses a semiconductor structure in which a diffusion region is formed in a silicon substrate and a polysilicon gate is formed on the top surface of the silicon substrate adjacent to, but not

contacting, the diffusion region. Ex. 1001, col. 3, ll. 1–6, 14–18. A layer of insulating material is then deposited on top of the polysilicon gate and the diffusion region. *Id*. at col. 3, ll. 6–7, 19–20. A via opening is formed in the insulating material to expose a portion of the polysilicon gate and a portion of the diffusion region. *Id*. at col. 3, ll. 7–8, 20–22. An electrically conducting material is deposited to at least partially fill the via opening to provide an electrical connection between the polysilicon gate and the diffusion region. *Id*. at col. 3, ll. 8–11, 23–27.

ILLUSTRATIVE CLAIM

> 7. A method of forming a local interconnect in a semiconductor structure, comprising the step of:
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> depositing an electrically conducting material in a via exposing at least a portion of a gate, a sidewall spacer adjacent to said gate and a portion of a diffusion region such that said electrically conducting material contacts and provides electrical communication between said gate and said diffusion region, said semiconductor structure comprising said diffusion region in a silicon substrate, said gate being on said substrate juxtaposed to but not contacting said diffusion region, said sidewall spacer being disposed above said diffusion region, said via being in an insulating material on said gate.

GROUNDS OF INSTITUTION

In our Decision to Institute, we instituted trial on the following challenges to patentability:

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