

# Exhibit C



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**Lee et al.**

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(54) **METHOD FOR FABRICATING A PACKAGING DEVICE FOR SEMICONDUCTOR DIE AND SEMICONDUCTOR DEVICE INCORPORATING SAME**

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(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(51) **Int. Cl.**  
**H01L 21/00** (2006.01)

(52) **U.S. Cl.** ..... **438/106; 438/125**

(58) **Field of Classification Search** ..... 438/106-107, 438/111-113, 116, 118-119, 121-127, 26; 361/719, 720, 767; 257/E21.067, 21.577, 257/21.585, 21.588; 174/265  
 See application file for complete search history.

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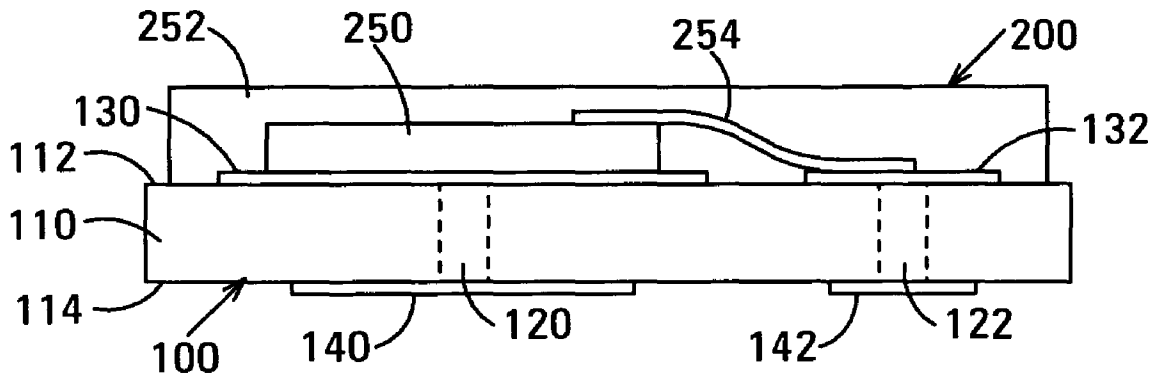
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Primary Examiner—Sara Crane

(57) **ABSTRACT**

A substantially planar substrate having opposed major surfaces is provided. The substrate includes a through hole that extends between the major surfaces. The through hole is filled with a conductive interconnecting element. A conductive mounting pad and a conductive connecting pad are formed on different ones of the major surfaces in electrical contact with the conductive interconnecting element. The packaging device formed by the method has a volume that is only a few times that of the semiconductor die and can be fabricated from materials that can withstand high-temperature die attach processes. The packaging device can be configured as the only packaging device used in the semiconductor device or as a submount for a semiconductor die that requires a high-temperature die attach process.

12 Claims, 8 Drawing Sheets



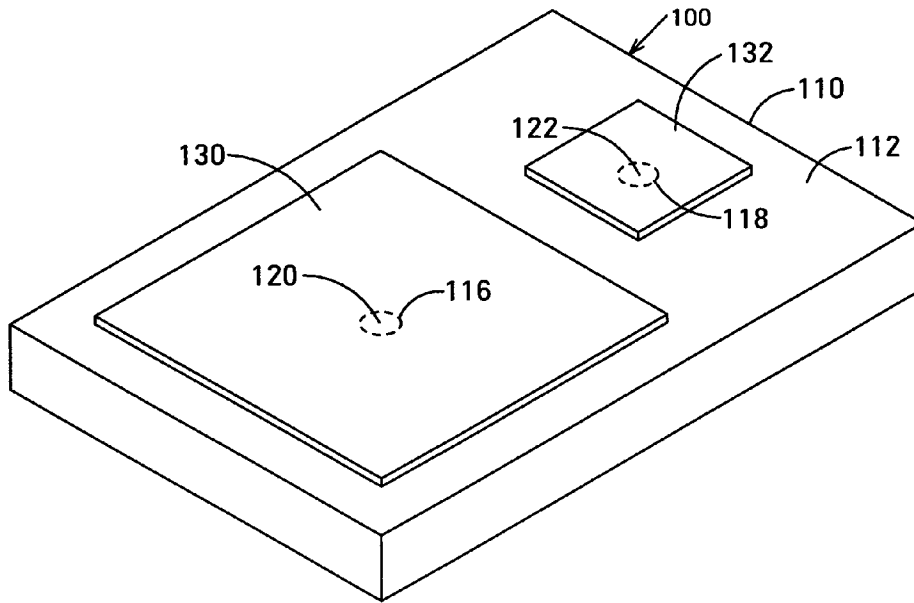


FIG. 1A

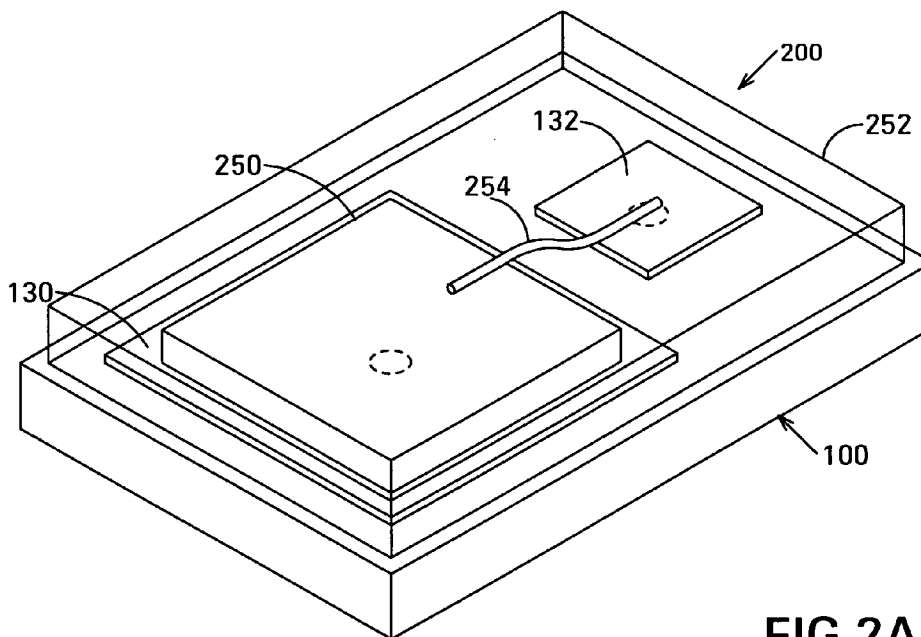


FIG. 2A

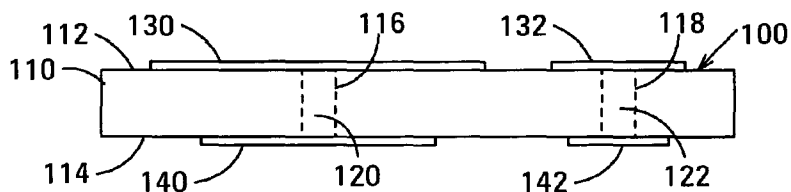


FIG. 1B

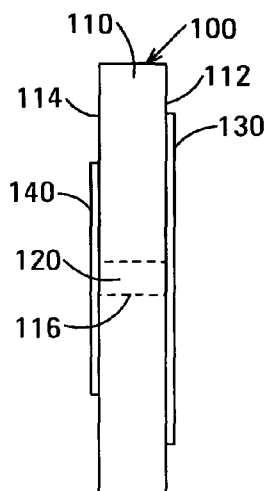


FIG. 1C

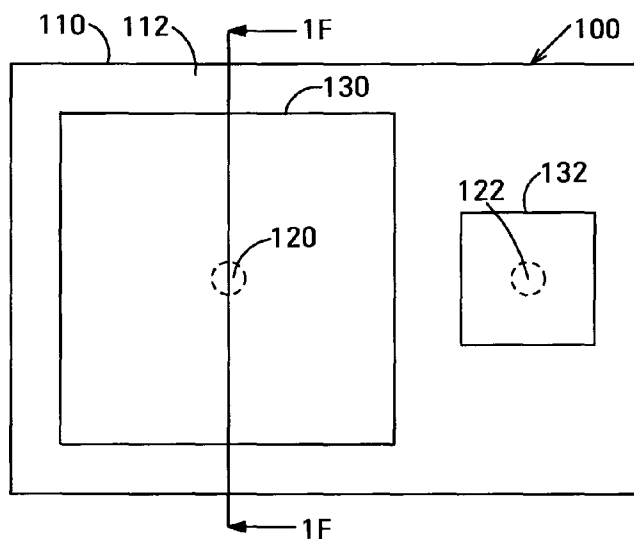


FIG. 1D

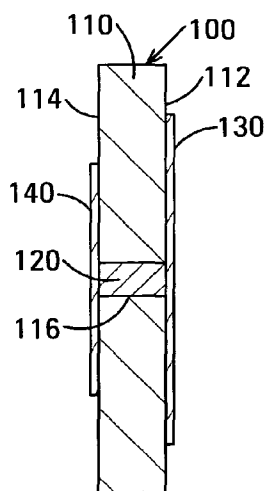


FIG. 1F

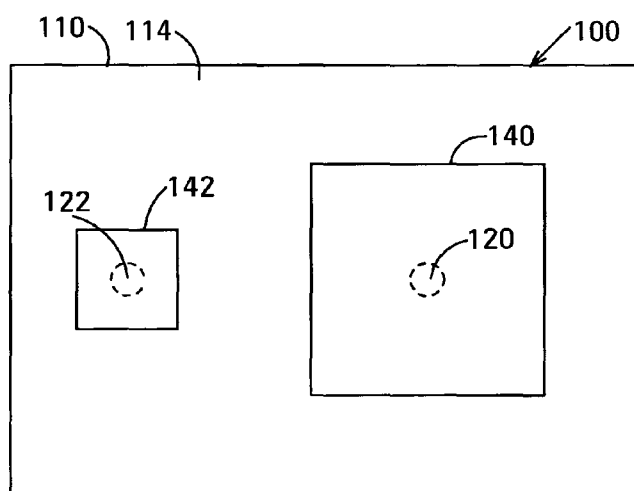


FIG. 1E

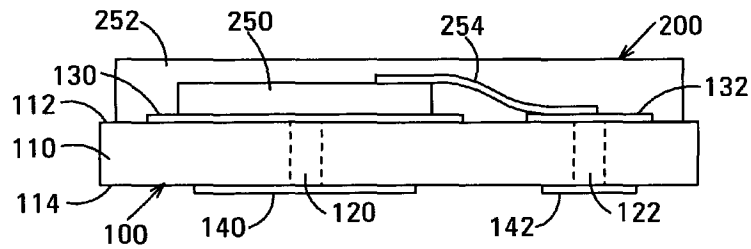


FIG. 2B

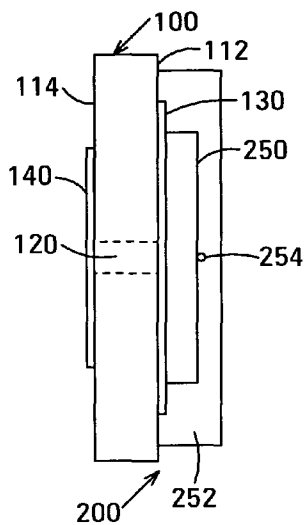


FIG. 2C

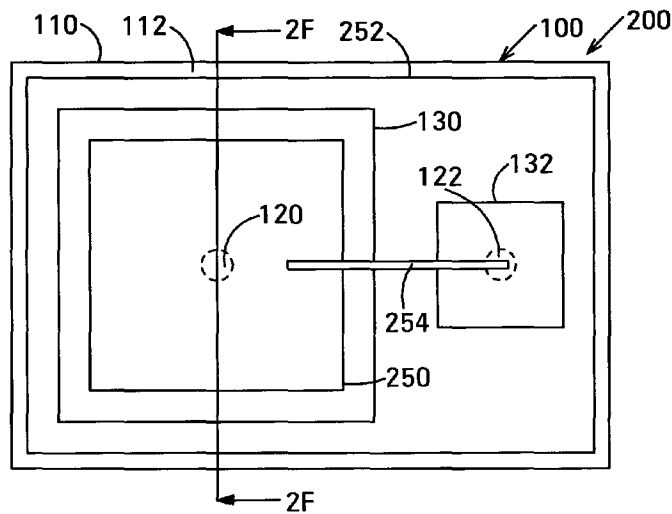


FIG. 2D

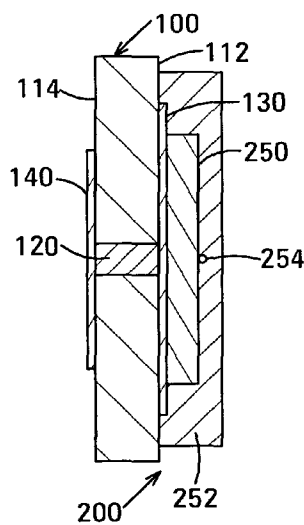


FIG. 2F

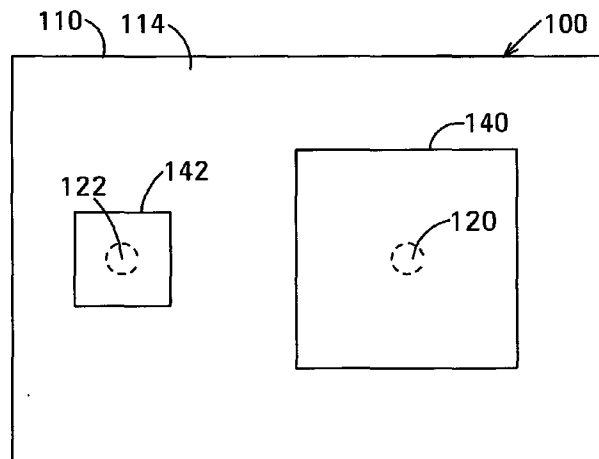


FIG. 2E

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